iPEM, ASYNC SRAM
16Mb, 512K x 32

Part Numbers: AS8S512K32PECB

Preliminary Data Sheet

The Micross Integrated Asynchronous Static Random Access memory component is manufactured utilizing (4) 4Mb, Asynchronous SRAMs integrated on an organic substrate with Lead-frame and encapsulated. The device is a High Speed, Power efficient random access memory device supporting parallel Byte, Word and Double Word accesses via use of multiple chip enables and is packaged in a manufacturing friendly surface mount PLCC footprint.

The Micross 16Mb SRAM iPEM operates from a single 5V supply, is TTL and CMOS compatible and is a fully static device requiring no clocks or memory cell refreshes to operate.

Features

General:
- Access Time: 12,15, 20 & 25ns
- Low Active Power: 1.55 watts (Typical)
- Low CMOS Standby Power: 400mW (Typical)
- Single 5V supply
- TTL compatible interface

Density and Organization:
- 16Mb, 512K x 32

Package:
- 68 Lead PLCC
- JEDEC MS-018, AE

Operating Voltage Range:
- VCC: 4.50V – 5.50V

Operating Temperature Range:
- -55°C to +125°C

Revision History

Revision	Description	Release Date
0.0	Initial Release, 16Mb, x32, Integrated Plastic Encapsulated, Asynchronous SRAM, packaged in PLCC, 68LD, MO-047AE	September, 2005
0.1	Updated Ordering information	January, 2009
0.2	Added Micross information	January 2010
0.3	Upgraded Document to “RELEASE” status, obsoleted PEC package due to pin-out errors, added PECA package with revised pin-out.	March 2011
1.0	68-PLCC Package mechanical revised, conforming to MS-018AE, New Micross Datasheet format and revision to ICC1, ICC2 and ICC3 and TELQX specification limit change	6/16/2021

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1.0 Preface

This Product document uses typographical conventions to assist the reader in understanding the content. This section will define the test formatting used in the rest of the document.

1.1 Text Usage

BOLD – indicates important information and table, figure, and chapter references.

BOLD ITALIC – designates Micross part number

< ….. > - indicates user-entered text or comments

1.2 Standard Definitions

ASYNC	Asynchronous
SRAM	Static Random Access Memory
V	Voltage
mA	milliamp
µA	microamp
ns	nanosecond
pF	picofarad
A	Address Bus
Ex	Chip Enable, Active Low, Byte 0, 1, 2 & 3
W	Write Enable, Active Low
G	Output Enable, Active Low
DQ	Data Bus, input and output
/IT	Industrial temperature range
/ET	Extended temperature range
/XT	Military temperature range

1.3 Technical Support

In the event you have questions and/or need for information beyond the scope of this document, you may contact Micross Components via the following methods:

Micross Website: https://www.micross.com/contact-us/sales-contacts/

2.0 Functional Description

The Micross AS8S512K32PECB is a high speed, 5V 16Mb multi-chip, integrated plastic encapsulated Asynchronous SRAM Microcircuit, supplied in the Industries PLCC, a J-leaded surface mount component. The device is available with access times of 12, 15, 20 and 25ns, creating a zero wait-state/latency, real-time memory solution. The high speed, 5V supply voltage and flexible control interface make the device ideal for all your real-time embedded computer memory requirements.

The device can be configured as a 512K x 32 with individual byte controls via use of E0\-E3\ or reconfigured as a 1M x 16 or 2M x 8 via use of the same Chip Enables in addition to the Write Enable (W\) and Output Enable (G\) controls.

The device provides a 50+ percent space savings when compared with four 512K x 8, 36 pin SOJ devices. In addition, the AS8S512K32 has only a 20pF capacitance load on the Address lines vs. approximately 30pF for the four 36LD SOJs.

3.0 Packages

Table 1. Packages

Package Type	Lead Count	Part Number
Plastic J-Lead	68	PECB

4.0 Applicable Quality Flows

Table 2. Applicable Quality Levels			
Micross Plastic iPEM Flow		**Part Number**	**Temp Range**
Options:	INDUSTRIAL	IT	-40°C - +85°C
	ENHANCED	ET	-40°C - +105°C
	MIL-TEMP	XT	-55°C - +125°C

5.0 Functional Block Diagram

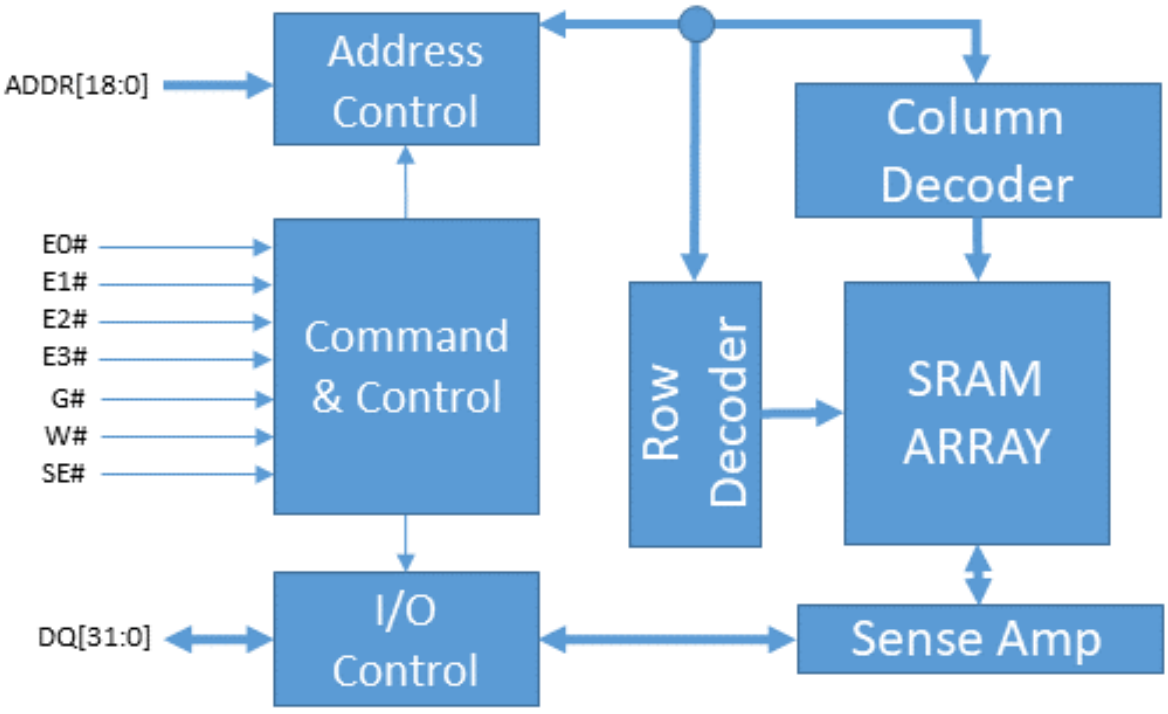

Figure 1. Functional Block Diagram

6.0 Performance Characteristics

Table 3. Performance Characteristics	
Parameter	**Value**
READ/WRITE MIN ACCESS TIMES	12ns
MAX OPERATING CURRENT	310mA
TTL STANDBY CURRENT	120mA
CMOS STANDBY CURRENT	80mA

7.0 Signal Descriptions

Table 4. Signal Descriptions		
Signal	**Type**	**Description**
E0\,E1\,E2\ & E3\	INPUT	Chip Enables, one per byte
W\	INPUT	Chip Enable
G\	INPUT	Output Enable
A[18:0]	INPUT	Addressable locations: 512K, 19 addresses
DQ[31:0]	I/O	Data Bus: 32 bit
VCC	SUPPLY	Core and I/O Positive Power supply
VSS	SUPPLY	Core and I/O Ground supply
NC		No Connects

8.0 Modes of Operation

Table 5. Mode of Operation								
Mode	**E0**	**E1**	**E2**	**E3**	**G#**	**W#**	**DQ[31:0]**	**Current**
Not Selected	H	H	H	H	X	X	HI-Z	I_{SB}
Output Disabled	L	L	L	L	H	H	HI-Z	I_{CC2}
READ BYTE 0	L	H	H	H	L	H	Data-Out	I_{CC1}
READ BYTE 1	H	L	H	H	L	H	Data-Out	I_{CC1}
READ BYTE 2	H	H	L	H	L	H	Data-Out	I_{CC1}
READ BYTE 3	H	H	H	L	L	H	Data-Out	I_{CC1}
READ WORD 0	L	L	H	H	L	H	Data-Out	I_{CC1}
READ WORD 1	H	H	L	L	L	H	Data-Out	I_{CC1}
READ DOUBLE WORD	L	L	L	L	L	H	Data-Out	I_{CC1}
WRITE BYTE 0	L	H	H	H	H	L	Data-In	I_{CC1}
WRITE BYTE 1	H	L	H	H	H	L	Data-In	I_{CC1}
WRITE BYTE 2	H	H	L	H	H	L	Data-In	I_{CC1}
WRITE BYTE 3	H	H	H	L	H	L	Data-In	I_{CC1}
WRITE WORD 0	L	L	H	H	H	L	Data-In	I_{CC1}
WRITE WORD 1	H	H	L	L	H	L	Data-In	I_{CC1}
WRITE DOUBLE WORD	L	L	L	L	H	L	Data-In	I_{CC1}

8.1 WRITE Operation

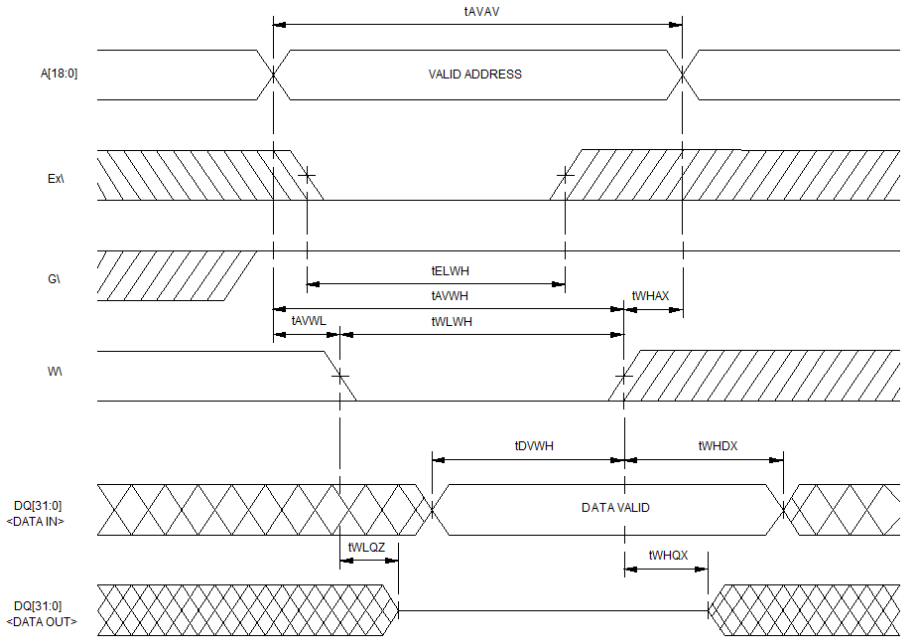

Figure 2. Write Operation (W# Controlled)

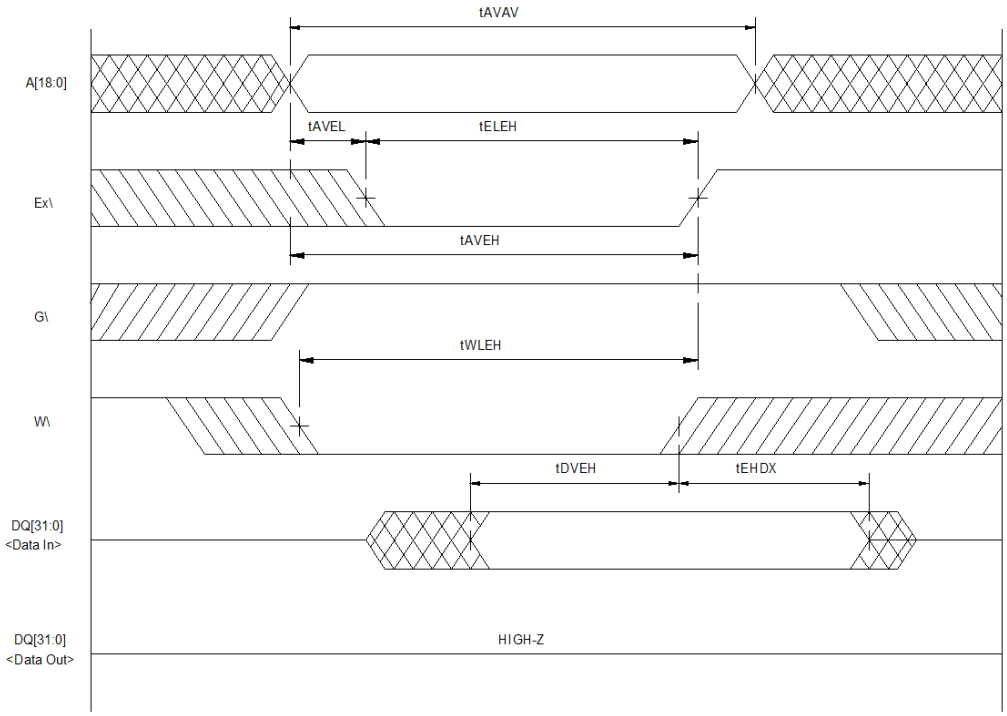

Figure 3. Write Operation (E# Controlled)

Table 6. WRITE Operation Timing										
Parameter	Symbol	12ns		15ns		205ns		25ns		Units
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE Cycle Time	tAVAV	12	-	15	-	20	-	25	-	ns
Chip Enable to End of Write	tELWH	8	-	10	-	11	-	12	-	ns
	tELEH	8	-	10	-	11	-	12	-	
Address Setup Time	tAVWL	0	-	0	-	0	-	0	-	ns
	tAVEL	0	-	0	-	0	-	0	-	
Address Valid to End of Write	tAVWH	8	-	10	-	11	-	12	-	ns
	tAVEH	8	-	10	-	11	-	12	-	
Write Pulse Width	tWLWH	8	-	10	-	11	-	12	-	ns
	tELEH	10	-	12	-	13	-	14	-	
Write Recovery Time	tWHAX	0	-	0	-	0	-	0	-	ns
	tEHAX	0	-	0	-	0	-	0	-	
Data Hold Time	tWHDX	0	-	0	-	0	-	0	-	ns
	tEHDX	0	-	0	-	0	-	0	-	
Write to Output in High Z	tWLQZ	0	6	0	7	0	8	0	9	ns
Data to Write Time	tDVWH	6	-	7	-	8	-	9	-	ns
	tDVEH	6	-	7	-	8	-	9	-	
Output Active from End of Write	tWHQX	3	-	3	-	3	-	3	-	ns

8.2 READ Operation

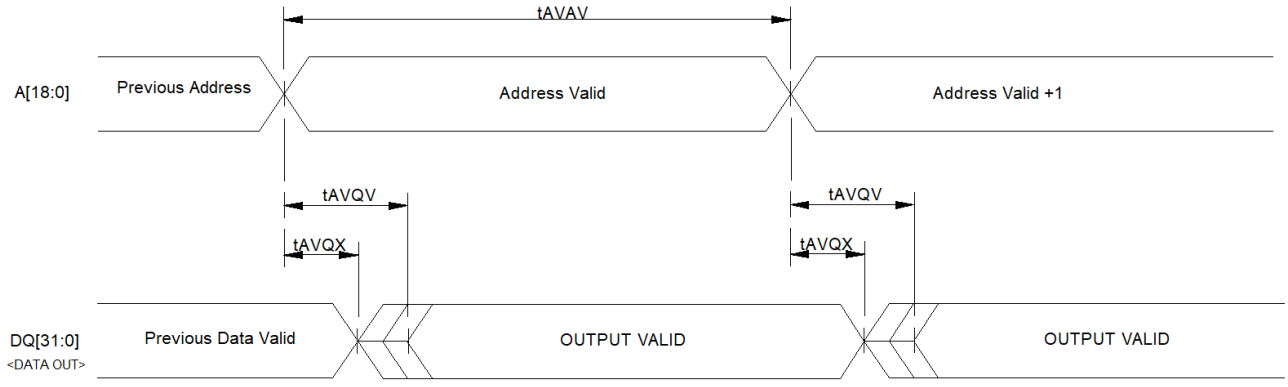

Figure 4. Continuous READ Operation

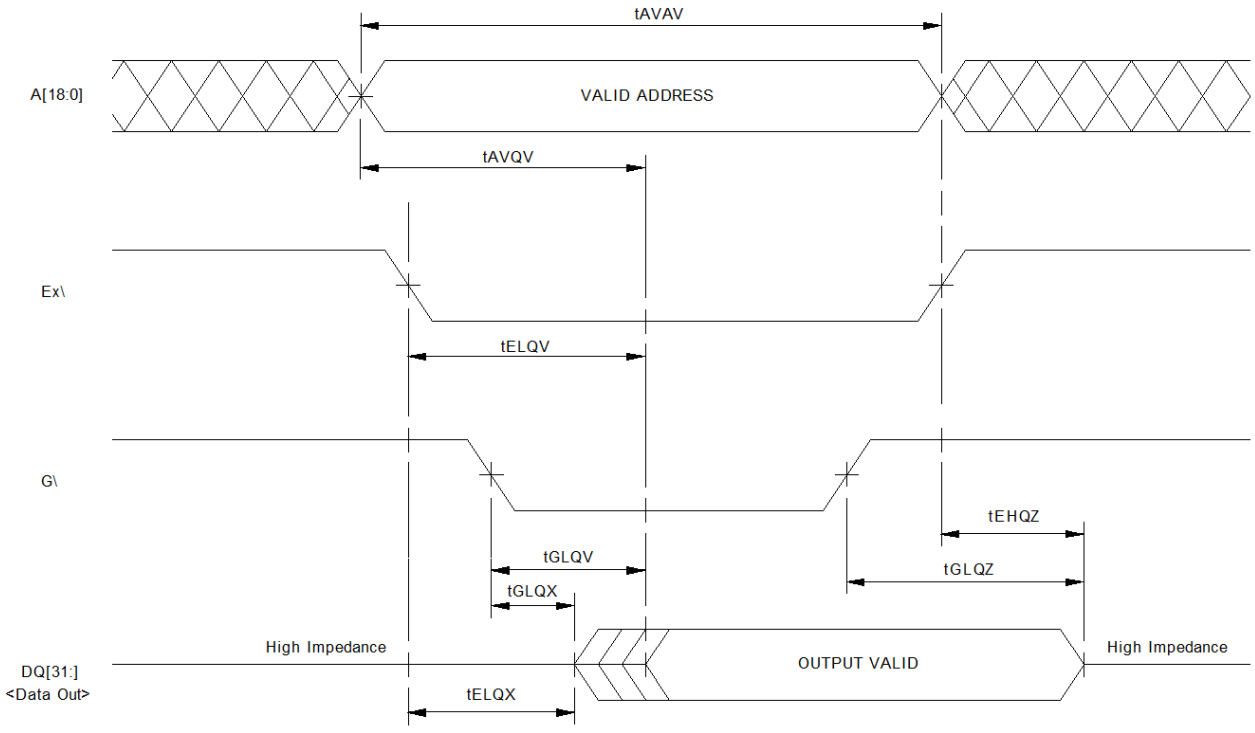

Figure 5. READ Operation, G\ Controlled

Table 7. READ Operation Timing										
Parameter	Symbol	12ns		15ns		20ns		25ns		Units
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ Cycle Time	tAVAV	12	-	15	-	20	-	25	-	ns
Address Cycle Time	tAVQV	-	12	-	15	-	20	-	25	ns
Chip Enable Access Time	tELQV	-	12	-	15	-	20	-	25	ns
Chip Enable to Output in Low Z	tELQX	2	-	2	-	2	-	2	-	ns
Chip Disable to Output in High Z	tEHQZ	-	6	-	6	-	6	-	6	ns
Output Hold from Address Change	tAVQX	3	-	3	-	3	-	3	-	ns
Output Enable to Output Valid	tGLQV	-	6	-	6	-	6	-	6	ns
Output Enable to Output Low Z	tGLQX	0	-	0	-	0	-	0	-	ns
Output Enable to Output High Z	tGHQZ	-	6	-	6	-	6	-	6	ns

9.0 Signal Pad Location

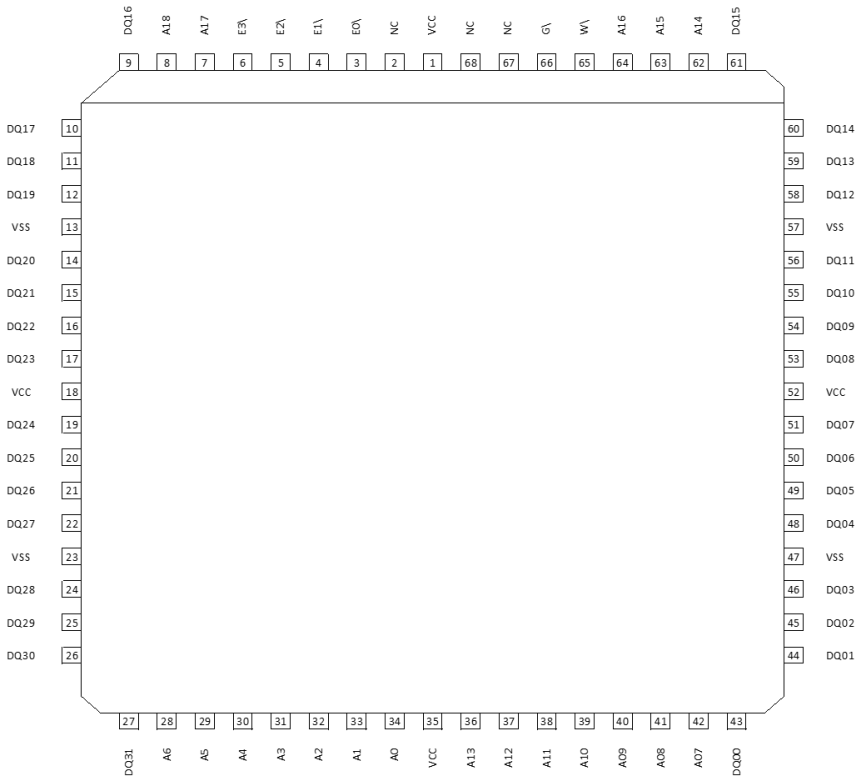

Figure 6. PLCC 68 Lead Signal Pad Location

Table 8. Package Size				
Package	**Package Type**	**Pin Count**	**Length**	**Width**
PLCC	PECB	68	0.990 INCH	0.990 INCH

Note: Package Outline Drawings on Page 17

10.0 Electrical Characteristics

Table 9. Absolute Maximum Ratings	
Voltage on any Pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature, t_A (Ambient)	
Industrial	-40°C to +85°C
Enhanced	-40°C to +105°C
Mil-Temp	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Power Dissipation	5.0 Watts
Output Current	20mA
Junction Temperature, T_J	175°C

Table 10. Recommended Operating Conditions						
Parameter	**Parameter/Test Conditions**	**Symbol**	**MIN.**	**TYP.**	**MAX.**	**Units**
SUPPLY VOLTAGE	5.0V Normal	V_{CC}	4.5	5	5.5	V
SUPPLY VOLTAGE	Digital GND	V_{SS}	0	0	0	V
INPUT HIGH VOLTAGE	INPUT LOGIC HIGH	V_{IH}	2.2	- -	V_{CC} + 0.5V	V
INPUT LOW VOLTAGE	INPUT LOGIC LOW	V_{IL}	-0.3	- -	0.8	V

Table 11. Capacitance						
Parameter	**Parameter/Test Conditions**	**Symbol**	**MIN.**	**TYP.**	**MAX.**	**Units**
Input Pin	TEMP = 25°C; f = 1MHz; V_{IN} = 0V	C_{IN}	-	-	20	pF
Input/Output	TEMP = 25°C; f = 1MHz; V_{IN} = 0V	C_{IO}	-	-	7	pF
W\, G\	TEMP = 25°C; f = 1MHz; VIN = 0V	CW, CG			20	pF
E0\,E1\.E2\ & E3\	TEMP = 25°C; f = 1MHz; VIN = 0V	CE			7	pF

Table 12. DC Characteristics						
Parameter	**Parameter/Test Conditions**	**Symbol**	**MIN.**	**TYP.**	**MAX.**	**Units**
Operating Current	VCC (max), I_{OUT} = 0 ma	I_{CC1}	-	-	310	mA
STANDBY Current	E# = V_{IH}, VCC (max)	I_{CC2}	-	-	120	mA
Full STANDBY Current	VCC (max), 125°C	I_{CC3}	-	-	80	mA
Input Leakage Current	V_{IN} = 0 to VCC (max)	I_{LI}	-5.0	-	5.0	µA
Output Leakage Current	V_{OUT} = 0 to VCC (max)	I_{LO}	-5.0	-	5.0	µA
Output HIGH Voltage	I_{OH} = -1.6mA	V_{OH}	2.4	-	-	V
Output LOW Voltage	I_{OL} = 1.6mA	V_{OL}	-	-	0.4	V

Table 13. AC Test Conditions	
Parameter	**Value**
Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	5ns
Input and Output timing levels	1.5V
Output load	FIGURE 11
Output load (tEHQZ, tGHQZ and tWLQZ)	FIGURE 12

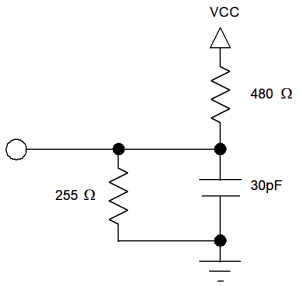

Figure 7. Output Load

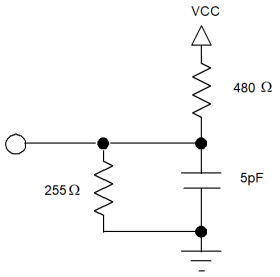

Figure 8. Output Load, High-Z

11.0 Package Outline Drawings

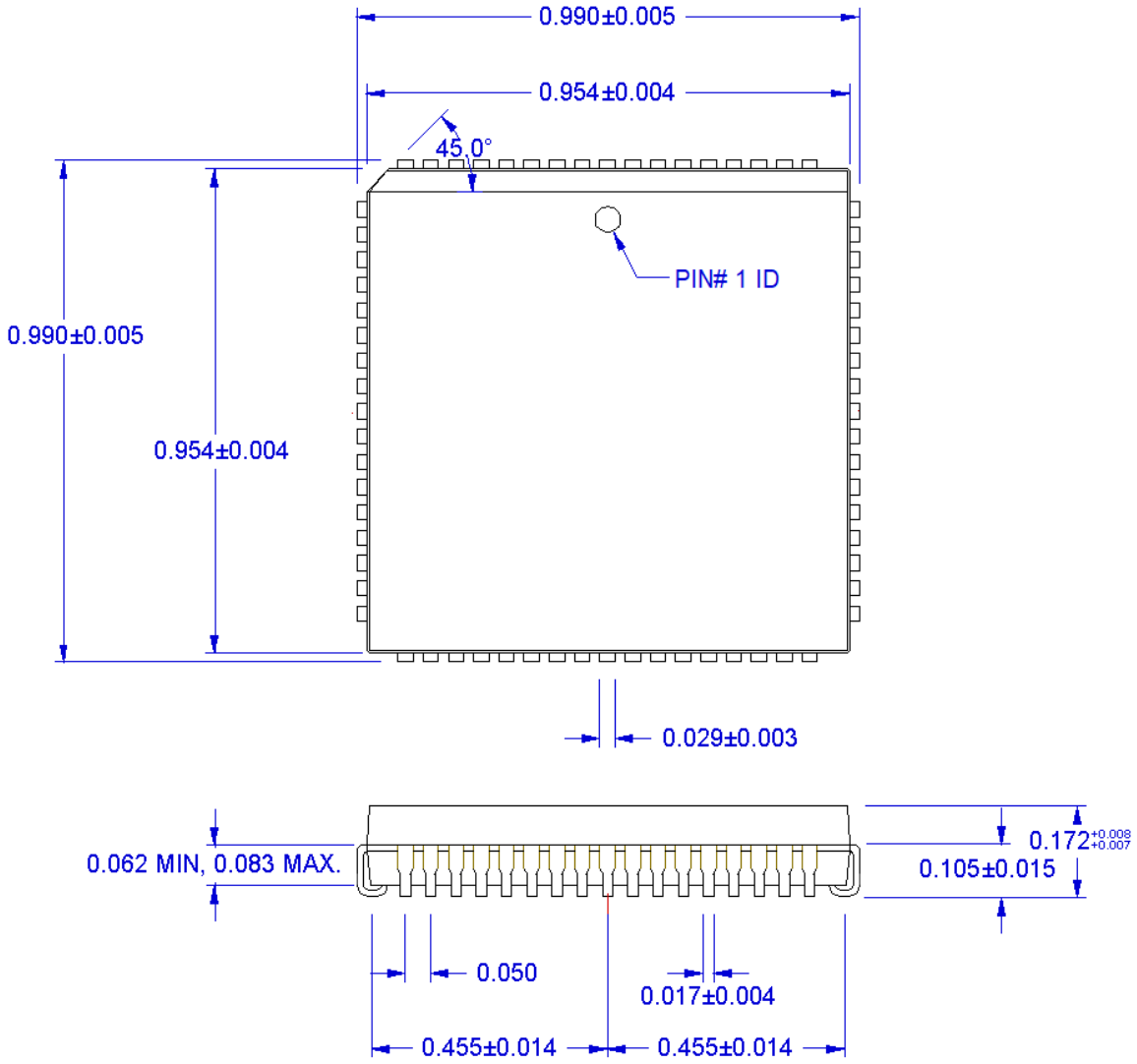

Figure 9. Plastic PLCC, 68 Lead, MS-018[AE]

12.0 Ordering Information

Table 14. Ordering Information			
Part Number	**Description**	**Package**	**Quality Level**
AS8S512K32PECA-12/IT	16Mb iPEM, 5V, 512K x 32, Async SRAM, 12ns	68-PLCC	Industrial
AS8S512K32PECA-15/IT	16Mb iPEM, 5V, 512K x 32, Async SRAM, 15ns	68-PLCC	Industrial
AS8S512K32PECA-20/IT	16Mb iPEM, 5V, 512K x 32, Async SRAM, 20ns	68-PLCC	Industrial
AS8S512K32PECA-25/IT	16Mb iPEM, 5V, 512K x 32, Async SRAM, 25ns	68-PLCC	Industrial
AS8S512K32PECA-12/ET	16Mb iPEM, 5V, 512K x 32, Async SRAM, 12ns	68-PLCC	Enhanced
AS8S512K32PECA-15/ET	16Mb iPEM, 5V, 512K x 32, Async SRAM, 15ns	68-PLCC	Enhanced
AS8S512K32PECA-20/ET	16Mb iPEM, 5V, 512K x 32, Async SRAM, 20ns	68-PLCC	Enhanced
AS8S512K32PECA-25/ET	16Mb iPEM, 5V, 512K x 32, Async SRAM, 25ns	68-PLCC	Enhanced
AS8S512K32PECA-12/XT	16Mb iPEM, 5V, 512K x 32, Async SRAM, 12ns	68-PLCC	Mil-Temp
AS8S512K32PECA-15/XT	16Mb iPEM, 5V, 512K x 32, Async SRAM, 15ns	68-PLCC	Mil-Temp
AS8S512K32PECA-20/XT	16Mb iPEM, 5V, 512K x 32, Async SRAM, 20ns	68-PLCC	Mil-Temp
AS8S512K32PECA-25/XT	16Mb iPEM, 5V, 512K x 32, Async SRAM, 25ns	68-PLCC	Mil-Temp

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