MYX6M4424

Dual 3A-Peak, Low-Side MOSFET Driver
Bipolar/CMOS/DMOS Process

General Description

The MYX6M4424 is based on Microchip/Micrel's MIC4424 silicon. The MYX6M4424 is a highly reliable, Military temperature BiCMOS/DMOS buffer/driver/MOSFET driver. It is a higher output current version of the MYX6M4427. The MYX6M4424 driver is capable of giving reliable service in more demanding electrical environments than its predecessor. The device will not latch under any conditions within its power and voltage rating. The MYX6M4424 can survive voltage noise/transient spikes up to 5V of either polarity, on the ground pin, as well as it can survive without either damage or logic upset, up to half an amp of reverse current (either polarity) forced back into their outputs.

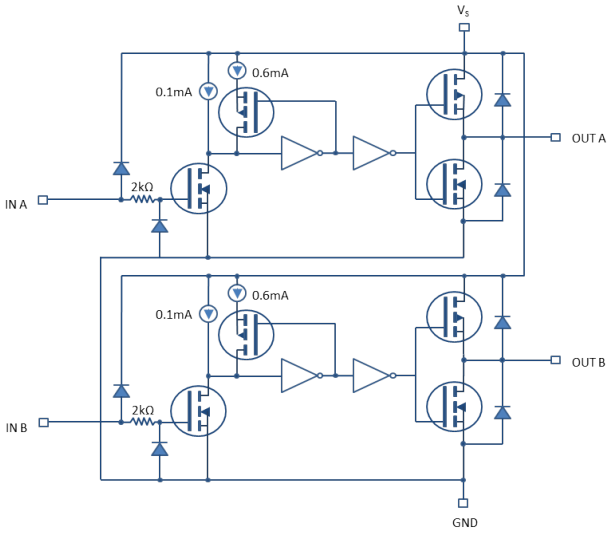
The MYX6M4424 driver is easier to use, more flexible in operation, and more forgiving than other CMOS or bipolar drivers currently available. The devices BiCMOS/DMOS construction dissipates minimum power and provides rail-to-rail voltage swings.

Primarily intended for driving power MOSFETs, the MYX6M4424 driver is suitable for driving other loads (capacitive, resistive, or inductive) which require low impedance, high peak currents, and fast switching times. Heavily loaded clock lines, coaxial cables, or piezoelectric transducers are some examples. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

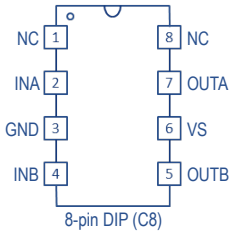
Features

- Non-Inverting Output
- Reliable, low-power bipolar/CMOS/DMOS construction
- Latch-up protected to >500mA reverse current
- Logic input withstands swing to –5V
- High 3A-peak output current
- Wide 4.5V to 18V operating range
- Drives 1800pF capacitance in 25ns
- Short <40ns typical delay time
- Delay times consistent with in supply voltage change
- Matched rise and fall times
- TTL logic input independent of supply voltage
- Low equivalent 6pF input capacitance
- Low supply current 3.5mA with logic-1 input
- 350µA with logic-0 input
- Low 3.5Ω typical output impedance
- Output voltage swings within 25mV of ground or V_S.
- '427', '1427', compatible pinout

Functional Block

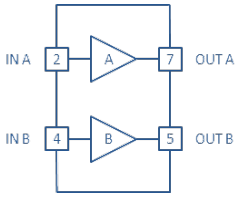


Pin Definition



8-pin DIP (C8)

Driver Configuration



Absolute Maximum Ratings

Supply Voltage ..... +22V
Input Voltage ..... VS + 0.3V to GND – 5V
Junction Temperature ..... 150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (10 sec.) ..... 300°C
ESD Susceptibility 1000V

Operating Ratings

Supply Voltage ..... +4.5V to +18V
Operating Temperature Range ..... -55°C to +125°C
Package Thermal resistance ..... 35°C/W

Ordering Information

PART NUMBER	SCREENING	PACKAGE	TEMP
MYX6M4424C8-XT	Mil-Temp	Ceramic, 8LD, SB-DIP	-55°C to +125°C
MYX6M4424C8-ET	Ext-Temp	Ceramic, 8LD, SB-DIP	-40°C to +105°C
MYX6M4424C8-IT	Ind-Temp	Ceramic, 8LD, SB-DIP	-40°C to +85°C

Application Information

Although the MYX6M4424 driver has been specifically constructed to operate reliably under any practical circumstances, there are nonetheless details of usage which will provide better operation of the device.

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging 2000pF from 0 to 15 volts in 20ns requires a constant current of 1.5A. In practice, the charging current is not constant, and will usually peak at around 3A. In order to charge the capacitor, the driver must be capable of drawing this much current, this quickly, from the system power supply. In turn, this means that as far as the driver is concerned, the system power supply must exhibit very low impedance.

As a practical matter, this means that the power supply bus must be bypassed in a heavy capacitive manner at the driver with at least 100X the load capacitance in order to achieve optimum driving speed. It also implies that the bypassing capacitor must have very low internal inductance and resistance at all frequencies of interest. Generally, this means using two capacitors, one a high-performance low ESR film, the other a low internal resistance ceramic, as together the valleys in their two impedance curves allow adequate performance over a broad enough band to get the job done. PLEASE NOTE that many film capacitors can be sufficiently inductive as to be useless for this service. Likewise, many multilayer ceramic capacitors have unacceptably high internal resistance. Use capacitors intended for high pulse current service.

The high pulse current demands of capacitive drivers also means that the bypass capacitors must be mounted very close to the driver in order to prevent the effects of lead inductance or PCB land inductance from nullifying what you are trying to accomplish. For optimum results the sum of the lengths of the leads and the lands from the capacitor body to the driver body should total 2.5cm or less.

Bypass capacitance, and its close mounting to the driver serves two purposes. Not only does it allow optimum performance from the driver, it minimizes the amount of lead length radiating at high frequency during switching, (due to the large ΔI) thus minimizing the amount of EMI later available for system disruption and subsequent cleanup. It should also be noted that the actual frequency of the EMI produced by a driver is not the clock frequency at which it is driven, but is related to the highest rate of change of current produced during switching, a frequency generally one or two orders of magnitude higher, and thus more difficult to filter if you let it permeate your system. Good bypassing practice is essential to proper operation of high speed driver ICs.

Grounding

Both proper bypassing and proper grounding are necessary for optimum driver operation. Bypassing capacitance only allows a driver to turn the load ON. Eventually (except in rare circumstances) it is also necessary to turn the load OFF. This requires attention to the ground path. Two things other than the driver affect the rate at which it is possible to turn a load off: The adequacy of the grounding available for the driver, and the inductance of the leads from the driver to the load. The latter will be discussed in a separate section.

Best practice for a ground path is obviously a well laid out ground plane. However, this is not always practical, and a poorly-laid out ground plane can be worse than none. Attention to the paths taken by return currents even in a ground plane is essential. In general, the leads from the driver to its load, the driver to the power supply, and the driver to whatever is driving it should all be as low in resistance and inductance as possible. Of the three paths, the ground lead from the driver to the logic driving it is most sensitive to resistance or inductance, and ground current from the load is what is most likely to cause disruption. Thus, these ground paths should be arranged so that they never share a land, or do so for as short a distance as is practical.

Output Lead Inductance

The same descriptions just given for PCB land inductance apply equally well for the output leads from a driver to its load, except that commonly the load is located much further away from the driver than the driver's ground bus.

Generally, the best way to treat the output lead inductance problem, when distances greater than 4cm (2") are involved, requires treating the output leads as a transmission line. Unfortunately, as both the output impedance of the driver and the input impedance of the MOSFET gate are at least an order of magnitude lower than the impedance of common coax, using coax is seldom a cost-effective solution. A twisted pair works about as well, is generally lower in cost, and allows use of a wider variety of connectors. The second wire of the twisted pair should carry common from as close as possible to the ground pin of the driver directly to the ground terminal of the load. Do not use a twisted pair where the second wire in the pair is the output of the other driver, as this will not provide a complete current path for either driver. Likewise, do not use

a twisted triad with two outputs and a common return unless both of the loads to be driver are mounted extremely close to each other, and you can guarantee that they will never be switching at the same time.

For output leads on a printed circuit, the general rule is to make them as short and as wide as possible. The lands should also be treated as transmission lines: i.e. minimize sharp bends, or changes in etchant width, as these will cause ringing. For a rough estimate, on a 1.59mm (0.062") thick G-10 PCB a pair of opposing lands each 2.36mm (0.093") wide translates to a characteristic impedance of about 50Ω. Half that width, or 1.18mm (0.046") suffices on a 0.787mm (0.031") thick PCB board. For accurate impedance matching with a MYX6M4424 driver, on a 1.59mm (0.062") board a land width of 42.75mm (1.683") would be required, due to the low impedance of the driver and (usually) its load. This is obviously impractical under most circumstances. Generally the tradeoff point between lands and wires comes when lands narrower than 3.18mm (0.125") would be required on a 1.59mm (0.062") board.

To obtain minimum delay between the driver and the load, it is considered best to locate the driver as close as possible to the load (using adequate bypassing). Using matching transformers at both ends of a piece of coax, or several matched lengths of coax between the driver and the load, works in theory, but is not optimum.

Driving at Controlled Rates

Occasionally there are situations where a controlled rise or fall time (which may be considerably longer than the normal rise or fall time of the driver's output) is desired for a load. In such cases it is still prudent to employ best possible practice in terms of bypassing, grounding and PCB layout, and then reduce the switching speed of the load (NOT the driver) by adding a non-inductive series resistor of appropriate value between the output of the driver and the load. For situations where only rise or only fall should be slowed, the resistor can be paralleled with a fast diode so that switching in the other direction remains fast. Due to the Schmitt-trigger action of the driver's input it is not possible to slow the rate of rise (or fall) of the driver's input signal to achieve slowing of the output.

Input Stage

The input stage of the MYX6M4424 consists of a single-MOSFET class A stage with an input capacitance of ≤38pF. This capacitance represents the maximum load from the driver that will be seen by its controlling logic. The drain load on the input MOSFET is a -2mA current source. Thus, the quiescent current drawn by the driver varies depending on the logic state of the input. Following the input stage is a buffer stage which provides ~400mV of hysteresis for the input, to prevent oscillations when slowly-changing input signals are used or when noise is present on the input. Input voltage switching threshold is approximately 1.5V which makes the driver directly compatible with TTL signals, or with CMOS powered from any supply voltage between 3V and 15V.

The MIC4423/24/25 drivers can also be driven directly by the SG1524/25/26/27, TL494/95, TL594/95, NE5560/61/62/68, TSC170, MIC38C42, and similar switch mode power supply ICs. By relocating the main switch drive function into the driver rather than using the somewhat limited drive capabilities of a PWM IC. The PWM IC runs cooler, which generally improves its performance and longevity, and the main switches switch faster, which reduces switching losses and increase system efficiency.

The input protection circuitry of the MYX6M4424, in addition to providing 2kV or more of ESD protection, also works to prevent latch up or logic upset due to ringing or voltage spiking on the logic input terminal. In most CMOS devices when the logic input rises above the power supply terminal, or descends below the ground terminal, the device can be destroyed or rendered inoperable until the power supply is cycled OFF and ON. The MYX6M4424 driver has been designed to prevent this. Input voltages excursions as great as 5V below ground will not alter the operation of the device. Input excursions above the power supply voltage will result in the excess voltage being conducted to the power supply terminal of the IC. Because the excess voltage is simply conducted to the power terminal, if the input to the driver is left in a high state when the power supply to the driver is turned off, currents as high as 30mA can be conducted through the driver from the input terminal to its power supply terminal. This may overload the output of whatever is driving the driver, and may cause other devices that share the driver's power supply, as well as the driver, to operate when they are assumed to be off, but it will not harm the driver itself. Excessive input voltage will also slow the driver down, and result in much longer internal propagation delays within the driver. TD2, for example, may increase to several hundred nanoseconds. In general, while the driver will accept this sort of misuse without damage, proper termination of the line feeding the driver, minimizing voltage spiking and ringing, will always result in faster and more reliable operation of the device and result in decreased EMI to be filtered out elsewhere, which also reduces stress to associated circuitry, minimizing unintended modes of operation.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as the 4000 series and 74Cxxx series devices have outputs which can only source or sink a few milliamps of current, and even shorting the output of the device to ground or VCC may not damage the device. CMOS drivers on the other hand, are intended to source or sink several Amps of current. This is necessary in order to drive large capacitive loads at frequencies into the megahertz range. Package power dissipation of driver ICs can easily be exceeded when driving large loads at high frequencies. Care must therefore be paid to device power dissipation when operating in this domain.

The supply current vs. frequency and supply current vs. load characteristic curves furnished here within the product datasheet, aid designers in estimating power dissipation in the driver. Operating frequency, power supply voltage and load conditions, all affect total power dissipation.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient temperature is easy to calculate.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load power dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 \times R_O \times D$$

Where:

I = the current drawn by the load
R_O = the output resistance of the driver when the output is high, at the power supply voltage used (see characteristic curves)
D = Duty Cycle

Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = \tfrac{1}{2} \times C \times V^2$$

As the energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the ½ is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = f \times C \times (V_S)2$$

Where:

f = Operating frequency
C = Load capacitance
V_S = Driver supply voltage

Inductive Load Power Dissipation

For inductive loads, the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$PL_1 = I^2 \times R_O \times D$$

However, in this instance, the RO required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected. This is only a part of the story which is to say calculation of the Inductive load properties is complicated by means that we have to calculate the inductive dissipation when forcing current through the driver and secondly, calculation when forcing current through the clamp diode, described by the formula:

$$PL_2 = I \times V_D (1 - D)$$

Where VD is the forward voltage drop across the clamp diode in the driver (generally around 0.70V). The two parts of the Inductive Load Dissipation must be summed to produce the total power dissipation (P_L).

$$PL = PL_1 + PL_2$$

Quiescent Power Dissipation

Quiescent power dissipation (PQ, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤2.0mA. Quiescent power can therefore be found from:

$$P_Q = V_S (D \times I_H + (1 - D) I_L)$$

Where:

I_H = Quiescent current with input high
I_L = Quiescent current with input low
D = Duty Cycle
V_S= Power Supply voltage

Transition Power Dissipation

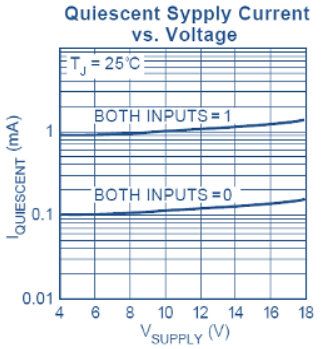
Transition power is dissipated in the driver each time its output change state because the transition, for a very brief interval, both the N and P-channel MOSFETs in the output totem-pole are ON simultaneously, causing a current conduction to occur briefly from VS to Ground. The transition power dissipation is approximately:

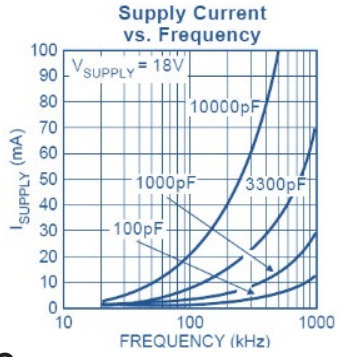
$$P_T = f \times V_S \times (A \times S)$$

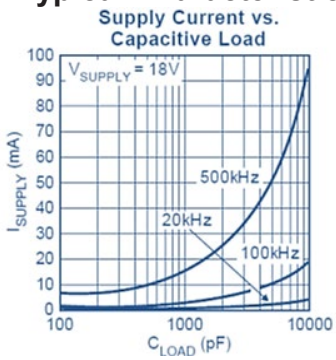
Where (A x S) is a time-current factor derived from the Crossover Energy Loss chart in relation to V_{IN} (see right side of page). Total power (PD) then, as previously described is just

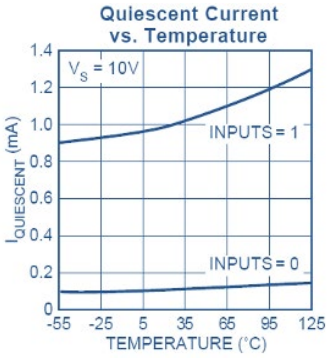
$$P_D = P_L + P_Q + P_T$$

Typical Characteristic Curves









MYX6M4424 Electrical Characteristics

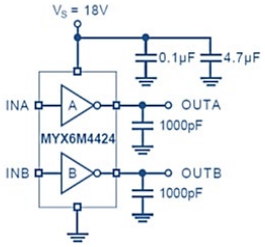
4.5V ≤ VS ≤ 18V; TA = -55°C ≤ TA ≤ 125°C

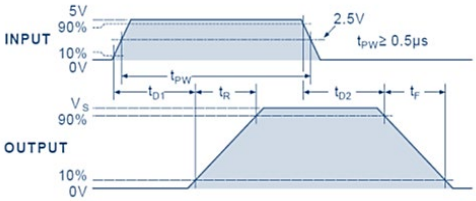
Parameter	Symbol	Test Conditions	Limits			Units	No
			Min.	Typ.	Max.		
Input							
Logic 1 Input	VIH		2.4	- -	- -	V	
Logic 0 Input	VIL		- -	- -	0.8	V	
Input Current	IIN	0V ≤ VIN ≤ Vs	-1	- -	1	µA	
		-5V ≤ VIN ≤ 0V	-10	- -	10		
Output							
Voltage Out HIGH	VOH	RL = ∞	VS - 25mV	- -	- -	V	
Voltage Out LOW	VOL	RL = ∞	- -	- -	25	mV	
Output Resistance HI State	RO1	IOUT = 10mA, VS = 18V	- -	- -	8	Ω	
Output Resistance LO State	RO2	IOUT = 10mA, VS = 18V	- -	- -	8	Ω	
Peak Output Current	IPK		- -	- -	3	A	
Supply							
Power Supply Current	IS1	VIN = 3.0V (both inputs)	- -	- -	2.5	mA	
	IS2	VIN = 0.0V (both inputs)	- -	- -	0.25		
Latch-up Protection	I		-500	- -	500	mA	
Switching							
Rise Time	tR	VS = 18V	- -	- -	35	nS	
Fall Time	tF	VS = 18V	- -	- -	35	nS	
Delay Time	tD1	VS = 18V	- -	- -	75	nS	
	tD2		- -	- -	75		

Notes

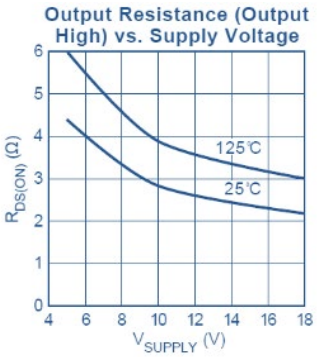
1. Guaranteed by Design
2. Tested Initially and after any design changes which may affect the performance of the device

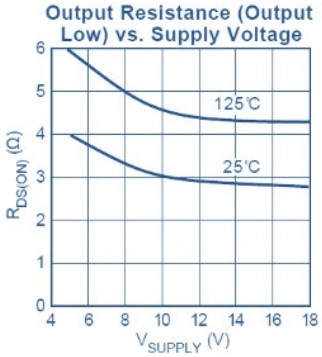
Switching Circuit

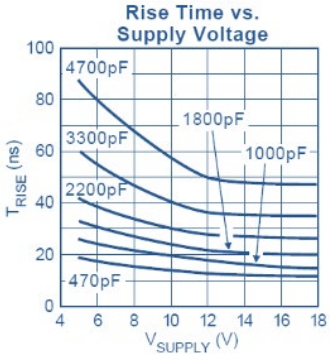


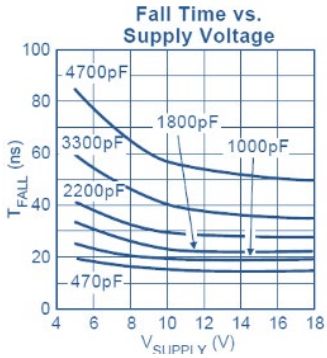


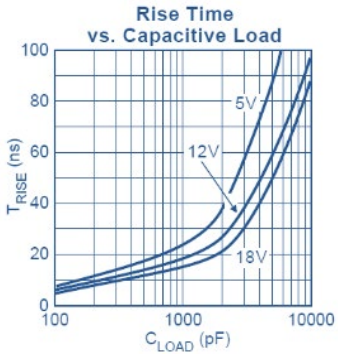
Typical Characteristic Curves – Continued

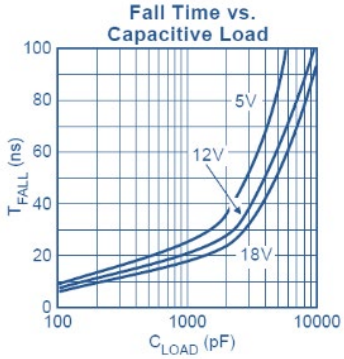


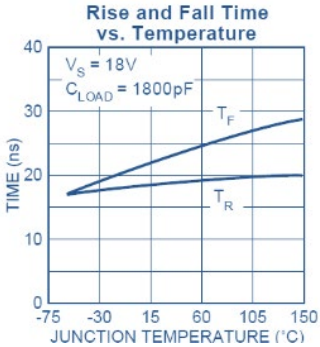


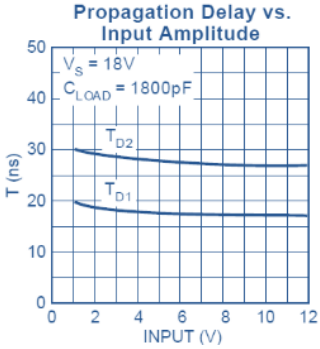




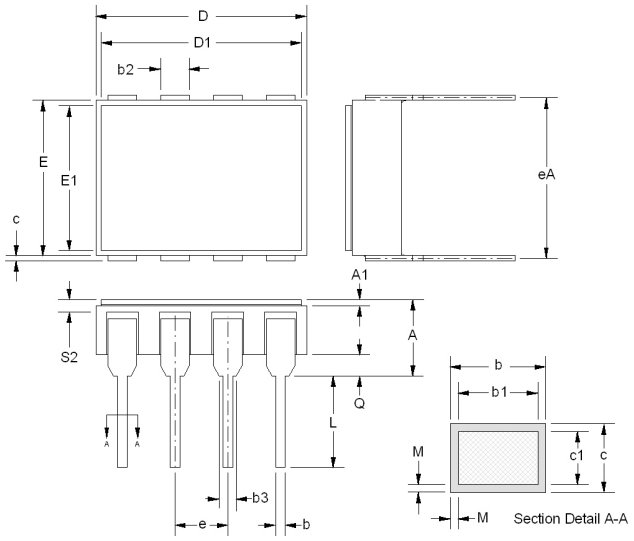








Mechanical Drawing



Dimensional	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	-	0.200	-	5.08
A1	0.011	0.013	0.28	0.33
b	0.014	0.026	0.36	0.66
b1	0.014	0.023	0.36	0.58
b2	0.045	0.065	1.14	1.65
b3	0.023	0.045	0.58	1.14
c	0.008	0.018	0.20	0.46
c1	0.008	0.015	0.20	0.38
D	-	0.405	-	10.29
D1	-	0.381	-	9.68
E	0.220	0.310	5.59	7.87
E1	0.210	0.300	5.33	7.62
e	0.100 BSC		2.54 BSC	
eA	0.300 BSC		7.62 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S2	0.005	-	0.13	-
M	-	0.0015	-	0.038