

1GByte DDR3 iPEM, Unbuffered Non-ECC – 128M x 64, ODT and Fly-By Address & Control Termination

Features

- Designed as small footprint, unbuffered, Non-ECC memory array in BGA
- $V_{CC} = 1.35V$
- Module Organization: 128M x 64
- Data path configuration: 64bit Non-ECC
- DDR3 Data rate: 800, 1066, 1333 Mbps
- Differential Clock Inputs
- Differential Data Strobe
- 8 internal banks for concurrent operation (per each 16bit word)
- 8n-bit prefetch architecture
- Auto & Self Refresh modes
- Nominal and Dynamic On-Die Termination (ODT)
- Fly-By-Termination for Address & Control
- Programmable CAS latency: 6, 7, 8, 9, 10, 11
- Posted CAS additive Latency: 0, 1, 2
- Selectable BC4 or BL8 on the Fly
- Write leveling
- Fixed Burst Length (BL)=8, and Burst Chop (BC)=4
- Programmable Write Latency: 5, 6, 7, 8 based on T_{CK}

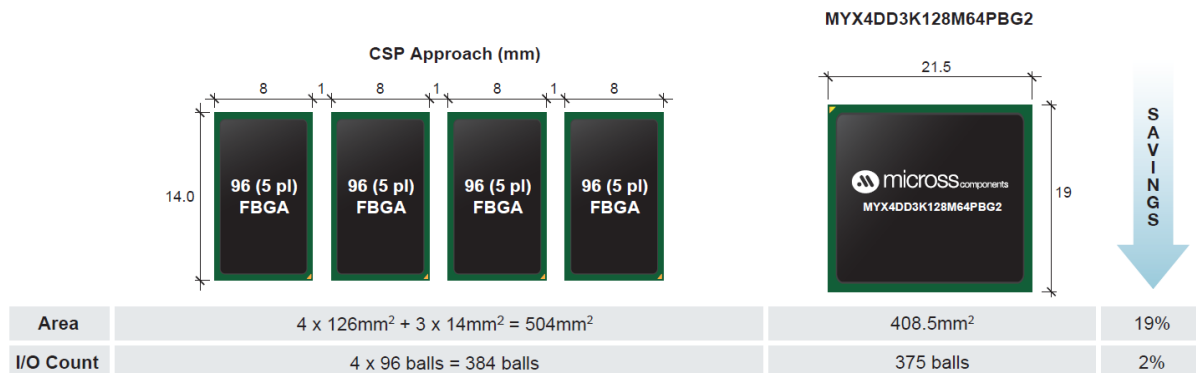
Benefits

- 19% space savings vs. Discrete FBGA approach
- 2% I/O reduction vs. Discrete FBGA approach
- Reduced part count and I/O reduction improves interconnect reliability of your memory array
- Reduced trace lengths for lower parasitic capacitance
- Suitable for Hi-Reliability applications
- Designed as SO-DIMM in BGA footprint with Fly-By-Termination, resulting in a robust, enhanced signal integrity solution
- Includes VTT, VREFCA and VREFDQ decoupling

Table 1: Product Availability

Part Number	Clock Frequency	Data Rate	Device Grade
MYX4DD3K128M64PBG2-25IT	400	800	Industrial
MYX4DD3K128M64PBG2-19IT	533	1066	
MYX4DD3K128M64PBG2-15IT	667	1333	
MYX4DD3K128M64PBG2-13IT	800	1600	Consult Factory
MYX4DD3K128M64PBG2-25ET	400	800	Enhanced
MYX4DD3K128M64PBG2-19ET	533	1066	
MYX4DD3K128M64PBG2-15ET	667	1333	
MYX4DD3K128M64PBG2-13ET	800	1600	Consult Factory
MYX4DD3K128M64PBG2-25XT	400	800	Mil-Temp
MYX4DD3K128M64PBG2-19XT	533	1066	
MYX4DD3K128M64PBG2-15XT	667	1333	

Figure 1: Footprint Space Comparisons



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Figure 2: 375-Ball PBGA (Top View, Ball Down)

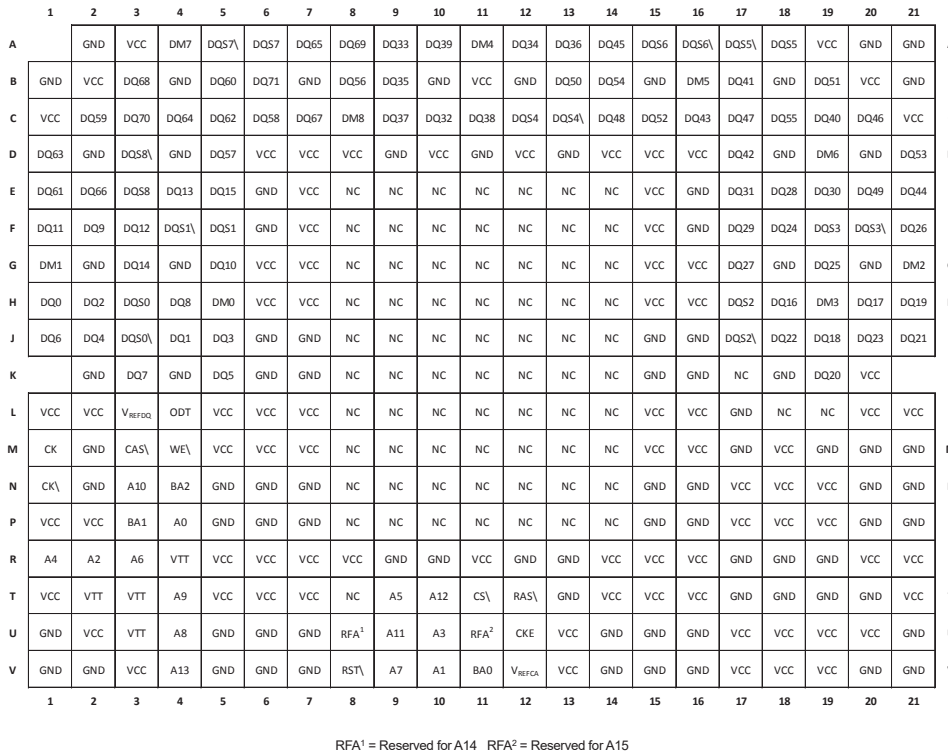


Figure 3: Functional Block Diagram

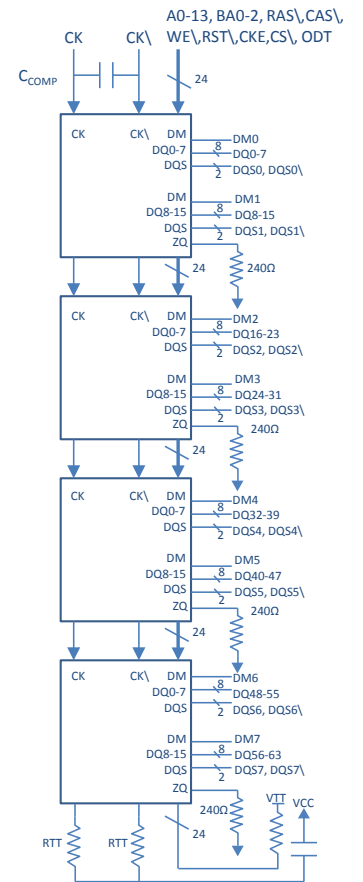


Figure 4: Mechanical

