

## 1GByte DDR3 iPEM, Unbuffered Non-ECC – 128M x 64, ODT and Fly-By Address & Control Termination

### Features

- Designed as small footprint, unbuffered, Non-ECC memory array in BGA
- $V_{CC} = 1.35V$
- Module Organization: 128M x 64
- Data path configuration: 64bit Non-ECC
- DDR3 Data rate: 800, 1066, 1333 Mbps
- Differential Clock Inputs
- Differential Data Strobe
- 8 internal banks for concurrent operation (per each 16bit word)
- 8n-bit prefetch architecture
- Auto & Self Refresh modes
- Nominal and Dynamic On-Die Termination (ODT)
- Fly-By-Termination for Address & Control
- Programmable CAS latency: 6, 7, 8, 9, 10, 11
- Posted CAS additive Latency: 0, 1, 2
- Selectable BC4 or BL8 on the Fly
- Write leveling
- Fixed Burst Length (BL)=8, and Burst Chop (BC)=4
- Programmable Write Latency: 5, 6, 7, 8 based on  $T_{CK}$

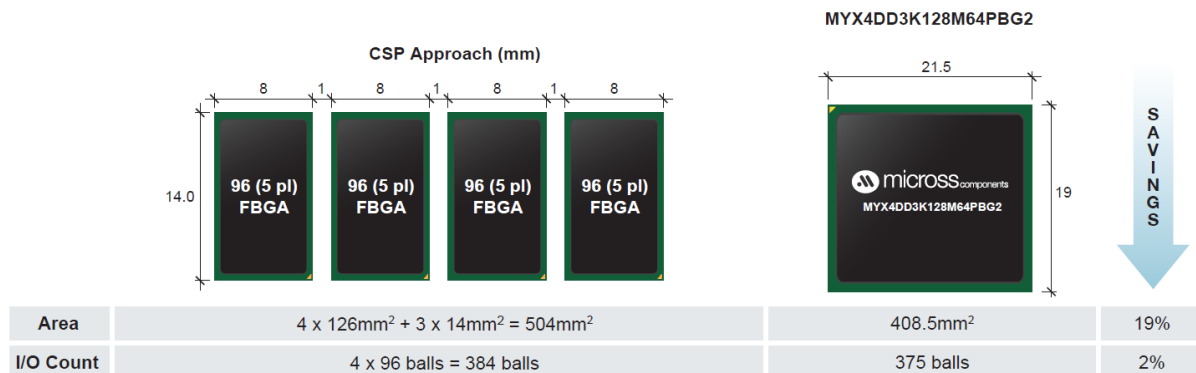
### Benefits

- 19% space savings vs. Discrete FBGA approach
- 2% I/O reduction vs. Discrete FBGA approach
- Reduced part count and I/O reduction improves interconnect reliability of your memory array
- Reduced trace lengths for lower parasitic capacitance
- Suitable for Hi-Reliability applications
- Designed as SO-DIMM in BGA footprint with Fly-By-Termination, resulting in a robust, enhanced signal integrity solution
- Includes VTT, VREFCA and VREFDQ decoupling

Table 1: Product Availability

Part Number	Clock Frequency	Data Rate	Device Grade
MYX4DD3K128M64PBG2-25IT	400	800	Industrial
MYX4DD3K128M64PBG2-19IT	533	1066	
MYX4DD3K128M64PBG2-15IT	667	1333	
MYX4DD3K128M64PBG2-13IT	800	1600	Consult Factory
MYX4DD3K128M64PBG2-25ET	400	800	Enhanced
MYX4DD3K128M64PBG2-19ET	533	1066	
MYX4DD3K128M64PBG2-15ET	667	1333	
MYX4DD3K128M64PBG2-13ET	800	1600	Consult Factory
MYX4DD3K128M64PBG2-25XT	400	800	Mil-Temp
MYX4DD3K128M64PBG2-19XT	533	1066	
MYX4DD3K128M64PBG2-15XT	667	1333	

Figure 1: Footprint Space Comparisons



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Figure 2: 375-Ball PBGA (Top View, Ball Down)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		
A		GND	VCC	DM7	DQ57	DQ57	DQ65	DQ69	DQ33	DQ39	DM4	DQ34	DQ36	DQ45	DQ56	DQ55	DQ55	VCC	GND	GND		A	
B		GND	VCC	DQ68	GND	DQ60	DQ71	GND	DQ56	DQ35	GND	VCC	GND	DQ50	DQ54	GND	DM5	DQ41	GND	DQ51	VCC	GND	B
C		VCC	DQ59	DQ70	DQ64	DQ62	DQ58	DQ67	DM8	DQ37	DQ32	DQ38	DQ54	DQ48	DQ52	DQ43	DQ47	DQ55	DQ40	DQ46	VCC		C
D		DQ63	GND	DQ58	GND	DQ57	VCC	VCC	VCC	GND	VCC	GND	VCC	VCC	VCC	DQ42	GND	DM6	GND	DQ53			D
E		DQ61	DQ66	DQ58	DQ13	DQ15	GND	VCC	NC	NC	NC	NC	NC	NC	VCC	GND	DQ31	DQ28	DQ30	DQ49	DQ44		E
F		DQ11	DQ9	DQ12	DQ51	DQ51	GND	VCC	NC	NC	NC	NC	NC	NC	VCC	GND	DQ29	DQ24	DQ53	DQ53	DQ26		F
G		DM1	GND	DQ14	GND	DQ10	VCC	VCC	NC	NC	NC	NC	NC	NC	VCC	VCC	DQ27	GND	DQ25	GND	DM2		G
H		DQ0	DQ2	DQ50	DQ8	DM0	VCC	VCC	NC	NC	NC	NC	NC	NC	VCC	VCC	DQ52	DQ16	DM3	DQ17	DQ19		H
J		DQ6	DQ4	DQ50	DQ1	DQ3	GND	GND	NC	NC	NC	NC	NC	NC	GND	GND	DQ52	DQ22	DQ18	DQ23	DQ21		J
K		GND	DQ7	GND	DQ5	GND	GND	NC	NC	NC	NC	NC	NC	NC	GND	GND	NC	GND	DQ20	VCC			K
L		VCC	VCC	V <sub>REFDQ</sub>	ODT	VCC	VCC	VCC	NC	NC	NC	NC	NC	NC	VCC	VCC	GND	NC	NC	VCC	VCC		L
M		CK	GND	CAS	WE	VCC	VCC	VCC	NC	NC	NC	NC	NC	NC	VCC	VCC	GND	VCC	GND	GND	GND		M
N		CK	GND	A10	BA2	GND	GND	GND	NC	NC	NC	NC	NC	NC	GND	GND	VCC	VCC	VCC	GND	GND		N
P		VCC	VCC	BA1	A0	GND	GND	GND	NC	NC	NC	NC	NC	NC	GND	GND	VCC	VCC	VCC	GND	GND		P
R		A4	A2	A6	VTT	VCC	VCC	VCC	VCC	GND	GND	VCC	GND	GND	VCC	VCC	GND	GND	GND	VCC	VCC		R
T		VCC	VTT	VTT	A9	VCC	VCC	VCC	NC	A5	A12	CS	RAS	GND	VCC	VCC	VCC	GND	GND	GND	VCC		T
U		GND	VCC	VTT	A8	GND	GND	GND	RFA <sup>1</sup>	A11	A3	RFA <sup>2</sup>	CKE	VCC	GND	GND	GND	VCC	VCC	VCC	VCC		U
V		GND	GND	VCC	A13	GND	GND	GND	RST	A7	A1	BA0	V <sub>REFCA</sub>	VCC	GND	GND	GND	VCC	VCC	VCC	GND		V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

RFA<sup>1</sup> = Reserved for A14 RFA<sup>2</sup> = Reserved for A15

Figure 3: Functional Block Diagram

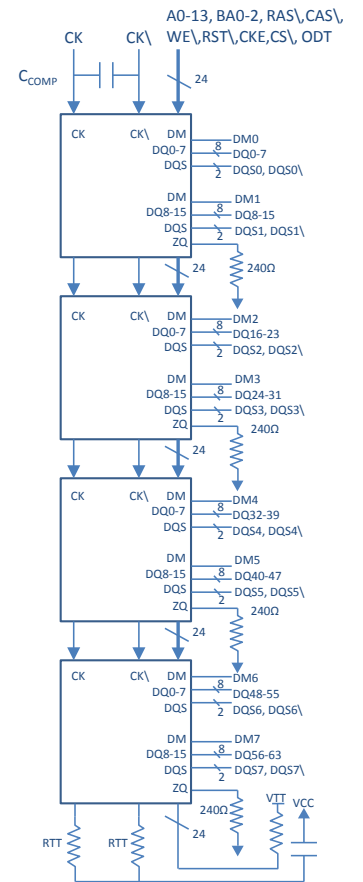


Figure 4: Mechanical

