- **Organization**
  512K × 16 Bits × 2 Banks
- **3.3-V Power Supply (±5% Tolerance)**
- **Two Banks for On-Chip Interleaving (Gapless Accesses)**
- **High Bandwidth – Up to 83-MHz Data Rates**
- **Read Latency Programmable to 2 or 3 Cycles From Column-Address Entry**
- **Burst Sequence Programmable to Serial or Interleave**
- **Burst Length Programmable to 1, 2, 4, 8, or 256 (Full Page)**
- **Chip Select and Clock Enable for Enhanced System Interfacing**
- **Cycle-by-Cycle DQ-Bus Mask Capability With Upper- and Lower-Byte Control**
- **Autorefresh Capability**
- **4K Refresh (Total for Both Banks)**
- **High-Speed, Low-Noise, Low-Voltage TTL (LVTTL) Interface**
- **Power-Down Mode**
- **Pipeline Architecture**
- **Temperature Ranges:**
  Operating, – 55°C to 125°C
  Storage, – 65°C to 150°C
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME t_{CK} (MIN)†	ACCESS TIME CLOCK TO OUTPUT t_{AC} (MIN)†	REFRESH TIME INTERVAL t_{REF} (MAX)
'626162-12	12 ns	8 ns	32 ms
'626162-15	15 ns	9 ns	32 ms
'626162-20	20 ns	10 ns	32 ms

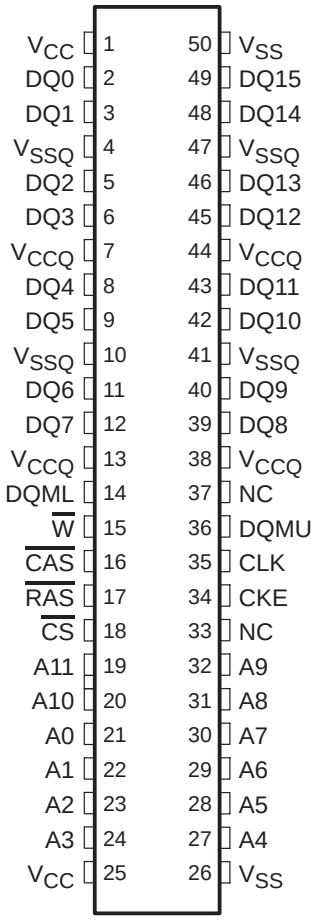
† Read latency = 3

description

The SMJ626162 series of devices are 16 777 216-bit synchronous dynamic random-access memory (SDRAM) devices organized as two banks of 524 288 words with 16 bits per word.

All inputs and outputs of the SMJ626162 series are compatible with the LVTTL interface.

HKD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A[0:10]	Address Inputs A0–A10 Row Addresses A0–A7 Column Addresses A10 Automatic-Precharge Select
A11	Bank Select
CAS	Column-Address Strobe
CKE	Clock Enable
CLK	System Clock
CS	Chip Select
DQ[0:15]	SDRAM Data Input/Data Output
DQML, DQMU	Data-Input/Data-Output Mask Enable
NC	No Connect
RAS	Row-Address Strobe
V_{CC}	Power Supply (3.3-V Typical)
V_{CCQ}	Power Supply for Output Drivers (3.3-V Typical)
V_{SS}	Ground
V_{SSQ}	Ground for Output Drivers
W	Write Enable

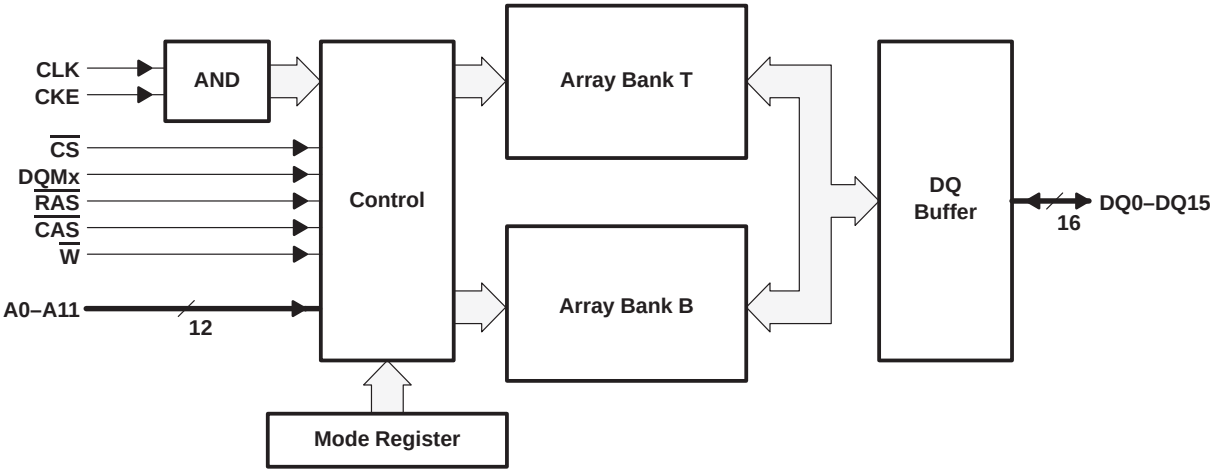
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

The SDRAM employs state-of-the-art technology for high performance, reliability, and low power requirements. All inputs and outputs are synchronized with the CLK input to simplify system design and enhance use with high-speed microprocessors and caches.

The SMJ626162 SDRAM is available in a 50-lead, 650-mil-wide ceramic dual flatpack (HKD suffix).

functional block diagram



operation

All inputs to the ’626162 SDRAM are latched on the rising edge of the system (synchronous) clock. The outputs, DQ0–DQ15, are also referenced to the rising edge of CLK. The ’626162 has two banks that are accessed independently; however, a bank must be activated before it can be accessed (read from or written to). Refresh cycles refresh both banks alternately.

Five basic commands or functions control most operations of the ’626162:

- Bank-activate/row-address entry
- Column-address entry/write operation
- Column-address entry/read operation
- Bank-deactivate
- Autorefresh

Additionally, operations can be controlled by three methods: using chip select ($\overline{CS}$) to select/deselect the devices, using DQMx to enable/mask the DQ signals on a cycle-by-cycle basis, or using CKE to suspend (or gate) the CLK input. The device contains a mode register that must be programmed for proper operation.

Table 1, Table 2, and Table 3 show the various operations that are available on the ’626162. These truth tables identify the command and/or operations and their respective mnemonics. Each truth table is followed by a legend that explains the abbreviated symbols. An access operation refers to any read or write command in progress at cycle n. Access operations include the cycle upon which the read or write command is entered and all subsequent cycles through the completion of the access burst.

operation (continued)

Table 1. Basic Command Truth Table†

COMMAND	STATE OF BANK(S)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A11	A10	A9 – A0	MNEMONIC
Mode register set	T = deac B = deac	L	L	L	L	X	X	A9 = V A8 – A7 = 0 A6 – A0 = V	MRS
Bank deactivate (precharge)	X	L	L	H	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	H	X	DCAB
Bank activate/row-address entry	SB = deac	L	L	H	H	BS	V	V	ACTV
Column-address entry / write operation	SB = actv	L	H	L	L	BS	L	V	WRT
Column-address entry / write operation with auto-deactivate	SB = actv	L	H	L	L	BS	H	V	WRT-P
Column-address entry/read operation	SB = actv	L	H	L	H	BS	L	V	READ
Column-address entry/read operation with auto-deactivate	SB = actv	L	H	L	H	BS	H	V	READ-P
No operation	X	L	H	H	H	X	X	X	NOOP
Control-input inhibit / no operation	X	H	X	X	X	X	X	X	DESL
Autorefresh‡	T = deac B = deac	L	L	L	H	X	X	X	REFR

† For execution of these commands on cycle n, one of the following must be true:
– CKE (n–1) must be high
– t_{CESP} must be satisfied for power-down exit
– t_{CES} and n_{CLE} must be satisfied for clock-suspend exit. DQMx (n) is irrelevant.

‡ Autorefresh entry requires that all banks be deactivated or be in an idle state prior to the command entry.

Legend:

n	=	CLK cycle number
L	=	Logic low
H	=	Logic high
X	=	Don't care, either logic low or logic high
V	=	Valid
T	=	Bank T
B	=	Bank B
actv	=	Activated
deac	=	Deactivated
BS	=	Logic high to select bank T; logic low to select bank B
SB	=	Bank selected by A11 at cycle n

operation (continued)

Table 2. Clock-Enable (CKE) Command Truth Table†

COMMAND	STATE OF BANK(S)	CKE (n – 1)	CKE (n)	$\overline{CS}$ (n)	$\overline{RAS}$ (n)	$\overline{CAS}$ (n)	$\overline{W}$ (n)	MNEMONIC
Power-down entry on cycle (n + 1)‡	T = no access operation§ B = no access operation§	H	L	X	X	X	X	PDE
Power-down exit¶	T = power down B = power down	L	H	X	X	X	X	—
CLK suspend on cycle (n + 1)	T = access operation§ B = access operation§	H	L	X	X	X	X	HOLD
CLK suspend exit on cycle (n + 1)	T = access operation§ B = access operation§	L	H	X	X	X	X	—

† For execution of these commands, A0 – A11 (n) and DQMx (n) are don't care entries.
‡ On cycle n, the device executes the respective command (listed in Table 1). On cycle (n + 1), the device enters power-down mode.
§ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.
¶ If setup time from CKE high to the next CLK high satisfies t_{CESP}, the device executes the respective command (listed in Table 1). Otherwise, either a DESL or a NOOP command must be applied before any other command.

Legend:
- n = CLK cycle number
- L = Logic low
- H = Logic high
- X = Don't care, either logic low or logic high
- T = Bank T
- B = Bank B

operation (continued)

Table 3. Data Mask (DQM) Command Truth Table†

COMMAND	STATE OF BANK(S)	DQML DQMU‡ (n)	DATA IN (n)	DATA OUT (n + 2)	MNEMONIC
—	T = deac and B = deac	X	N/A	Hi-Z	—
—	T = actv and B = actv (no access operation)§	X	N/A	Hi-Z	—
Data-in enable	T = write or B = write	L	V	N/A	ENBL
Data-in mask	T = write or B = write	H	M	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	V	ENBL
Data-out mask	T = read or B = read	H	N/A	Hi-Z	MASK

† For execution of these commands on cycle n, one of the following must be true:
– CKE (n) must be high
– t_{CESP} must be satisfied for power-down exit
– t_{CES} and n_{CLE} must be satisfied for clock-suspend exit.
$\overline{CS}$(n), $\overline{RAS}$(n), $\overline{CAS}$(n), $\overline{W}$(n), and A0 – A11 are irrelevant.

‡ DQML controls DQ0 – DQ7.
DQMU controls DQ8 – DQ15.

§ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.

Legend:

n	=	CLK cycle number
L	=	Logic low
H	=	Logic high
X	=	Don't care, either logic low or logic high
V	=	Valid
M	=	Masked input data
N/A	=	Not applicable
T	=	Bank T
B	=	Bank B
actv	=	Activated
deac	=	Deactivated
write	=	Activated and accepting data in on cycle n
read	=	Activated and delivering data out on cycle (n + 2)
Hi-Z	=	High-impedance state

burst sequence

All data for the ’626162 is written or read in a burst fashion—that is, a single starting address is entered into the device and then the ’626162 internally accesses a sequence of locations based on that starting address. Some of the subsequent accesses after the first access can be at preceding, as well as succeeding, column addresses, depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst (see Table 4, Table 5, and Table 6). The length of the burst can be programmed to be either 1, 2, 4, 8, or full-page (256) accesses (see the section on setting the mode register). After a read burst is completed (as determined by the programmed burst length), the outputs are in the high-impedance state until the next read access is initiated.

Table 4. 2-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A0			
	DECIMAL		BINARY	
	START	2ND	START	2ND
Serial	0	1	0	1
	1	0	1	0
Interleave	0	1	0	1
	1	0	1	0

Table 5. 4-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A1–A0							
	DECIMAL				BINARY			
	START	2ND	3RD	4TH	START	2ND	3RD	4TH
Serial	0	1	2	3	00	01	10	11
	1	2	3	0	01	10	11	00
	2	3	0	1	10	11	00	01
	3	0	1	2	11	00	01	10
Interleave	0	1	2	3	00	01	10	11
	1	0	3	2	01	00	11	10
	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00

burst sequence (continued)

Table 6. 8-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A2–A0															
	DECIMAL								BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Serial	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
Interleave	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101
	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

latency

The beginning data-out cycle of a read burst can be programmed to occur 2 or 3 CLK cycles after the read command (see the section on setting the mode register). This feature allows the adjustment of the ’626162 to operate in accordance with the system’s capability to latch the data output from the ’626162. The delay between the READ command and the beginning of the output burst is known as *read latency* (also known as CAS latency). After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum read latencies is restricted, based on the particular maximum frequency rating of the ’626162.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. The write latency is fixed and is not determined by the contents of the mode register.

two-bank operation

The ’626162 contains two independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Then, each bank must be deactivated before it can be activated again with a new row address. The bank-activate/row-address-entry command (ACTV) is entered by holding $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ high, $\overline{\text{W}}$ high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ-P or a WRT-P command or by use of the deactivate-bank command (DEAC). Both banks can be deactivated at once by use of the DCAB command (see Table 1 and the section on bank deactivation).

two-bank row-access operation

The two-bank feature allows access of information on random rows at a higher rate of operation than is possible with a standard DRAM. This is accomplished by activating one bank with a row address and, while the data stream is being accessed to/from that bank, activating the second bank with another row address. When the data stream to/from the first bank is complete, the data stream to/from the second bank can begin without interruption. After the second bank is activated, the first bank can be deactivated to allow the entry of a new row address for the next round of accesses. In this manner, operation can continue in an interleaved fashion. Figure 25 is an example of two-bank, row-interleaving, read bursts with automatic deactivate for a read latency of 3 and a burst length of 8.

two-bank column-access operation

The availability of two banks allows the access of data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), A11 can be used to alternate read or write commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Figure 26 is an example of two-bank, column-interleaving, read bursts for a read latency of 3 and a burst length of 2.

bank deactivation (precharge)

Both banks can be deactivated (placed in precharge) simultaneously by using the DCAB command. A single bank can be deactivated by using the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A11 is used to select the bank to be precharged as shown in Table 1. A bank can also be deactivated automatically by using A10 during a read or write command. If A10 is held high during the entry of a read or write command, the accessed bank (selected by A11) is deactivated automatically upon completion of the access burst. If A10 is held low during the entry of a read or write command, that bank remains active following the burst. The read and write commands with automatic deactivation are denoted as READ-P and WRT-P.

chip select ($\overline{CS}$)

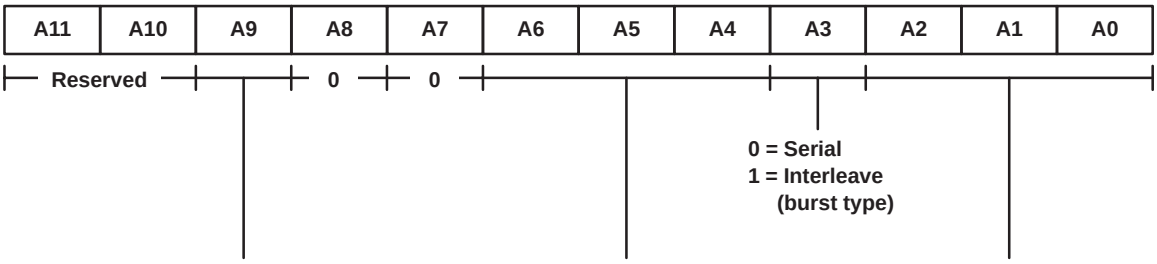
$\overline{CS}$ can be used to select or deselect the ’626162 for command entry, which might be required for multiple-memory-device decoding. If $\overline{CS}$ is held high on the rising edge of CLK (DESL command), the device does not respond to $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ until the device is selected again. Device select is accomplished by holding $\overline{CS}$ low on the rising edge of CLK. Any other valid command can be entered simultaneously on the same rising CLK edge of the select operation. The device can be selected/deselected on a cycle-by-cycle basis (see Table 1 and Table 2). The use of $\overline{CS}$ does not affect an access burst that is in progress; the DESL command can restrict only $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ input to the ’626162.

data mask

The mask command, or its opposite, the data-in enable (ENBL) command (see Table 3), is performed on a cycle-by-cycle basis to gate any individual data cycle within a read burst or a write burst. DQML controls DQ0–DQ7, and DQMU controls DQ8–DQ15. The application of DQMx to a write burst has no latency (n_{DID} = 0 cycle), but the application of DQMx to a read burst has a latency of n_{DOD} = 2 cycles. During a write burst, if DQMx is held high on the rising edge of CLK, the data-input is ignored on that cycle. During a read burst, if DQMx is held high on the rising edge of CLK, then n_{DOD} cycles after the rising edge of CLK, the data-output will be in the high-impedance state. Figure 16, Figure 29, Figure 30, Figure 31, and Figure 32 show examples of data-mask operations.

setting the mode register

The ’626162 contains a mode register that must be programmed with the read latency, the burst type, and the burst length. This is accomplished by executing a mode-register set (MRS) command with the information entered on address lines A0–A9. A logic 0 must be entered on A7 and A8. A10 and A11 are don’t care entries for the ’626162. When A9 = 1, the write-burst length is always 1. When A9 = 0, the write-burst length is defined by A0–A2. Figure 1 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ low and the input-mode word valid on A0–A9 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.



REGISTER BIT A9	WRITE-BURST LENGTH
0	A2–A0
1	1

REGISTER BITS†			READ LATENCY‡
A6	A5	A4	
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

REGISTER BITS†			BURST LENGTH
A2	A1	A0	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	1	1	256

† All other combinations are reserved.
‡ See the timing requirements for minimum valid read latencies based on maximum frequency rating.

Figure 1. Mode-Register Programming

refresh

The ’626162 must be refreshed at intervals not exceeding t_{REF} (see timing requirements) or data cannot be retained. Refresh can be accomplished by performing a read or write access to every row in both banks, or by performing 4096 autorefresh (REFR) commands. Regardless of the method used, refresh must be accomplished before t_{REF} has expired.

autorefresh (REFR)

Before performing a REFR operation, both banks must be deactivated (placed in precharge). To enter a REFR command, $\overline{RAS}$ and $\overline{CAS}$ must be low and $\overline{W}$ must be high upon the rising edge of CLK (see Table 1). The refresh address is generated internally such that after 4096 REFR commands, both banks of the ’626162 have been refreshed. The external address and bank select (A11) are ignored. The execution of a REFR command automatically deactivates both banks upon completion of the internal autorefresh cycle. This allows consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before t_{REF} expires.

CLK-suspend/power-down mode

For normal device operation, CKE must be held high to enable CLK. If CKE goes low during the execution of a read or write operation, the DQ bus occurring at the immediate next rising edge of CLK is frozen at its current state. No further inputs are accepted until CKE returns high; this is known as a CLK-suspend operation, and its execution is denoted as a HOLD command. The device resumes operation from the point at which it was placed in suspension, beginning with the second rising edge of CLK after CKE returns high.

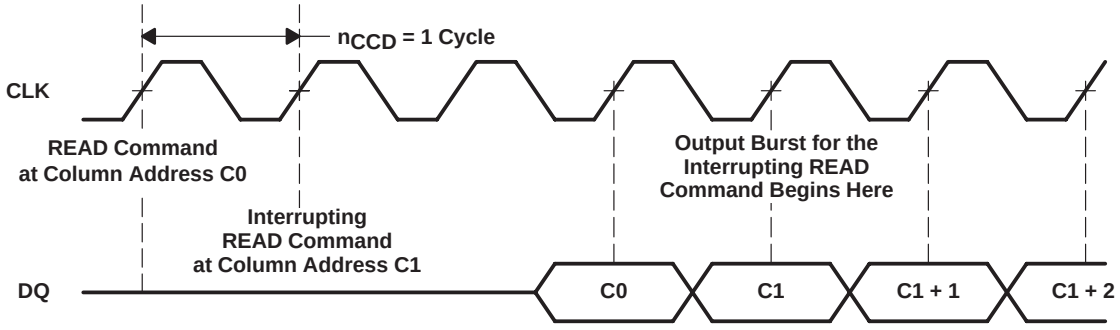
If CKE is brought low when no read or write command is in progress, the device enters the power-down mode. If both banks are deactivated when the power-down mode is entered, power consumption is reduced to the minimum. Power-down mode can be used during row-active or autorefresh periods to reduce input-buffer power. After power-down mode is entered, no further inputs are accepted until CKE returns high. To ensure that data in the device remains valid, the power-down mode must be exited periodically to meet the requirements described earlier for device refresh. When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time (t_{CESP}) is satisfied. Table 2 shows the command configuration for a CLK-suspend/power-down operation; Figure 17, Figure 18, and Figure 35 show examples of the procedure.

interrupted bursts

A read burst or write burst can be interrupted before the burst sequence has been completed with no adverse effects to the operation. This is accomplished by entering certain superseding commands as listed in Table 7 and Table 8, provided that all timing requirements are met. A DEAC command is considered an interrupt only if it is issued to the same bank as the preceding READ or WRT command. The interruption of a READ-P or a WRT-P operation is not supported.

Table 7. Read-Burst Interruption

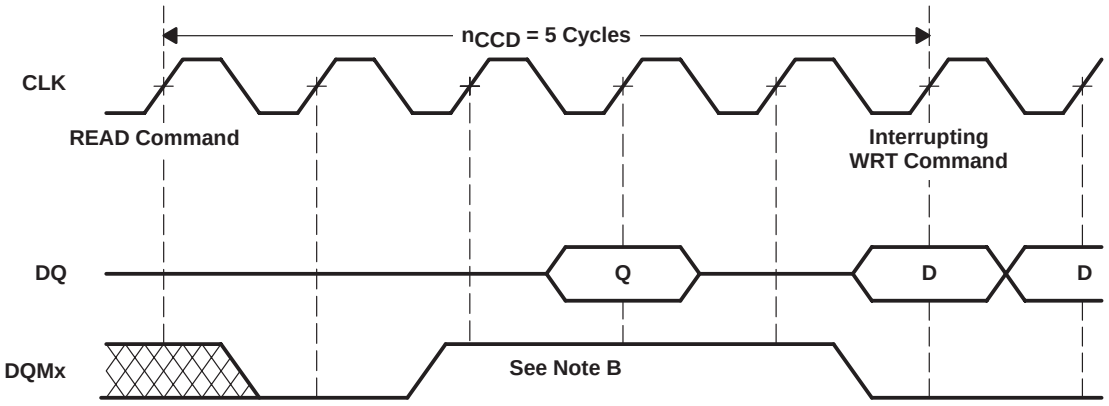
INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
READ, READ-P	Current output cycles continue until the programmed latency from the superseding READ (READ-P) command is met and new output cycles begin (see Figure 2).
WRT, WRT-P	The WRT (WRT-P) command immediately supersedes the read burst in progress. To avoid data contention, DQMx must be held high before the WRT (WRT-P) command to mask output of the read burst on cycles (n_{CCD}–1), n_{CCD}, and (n_{CCD}+1), assuming that there is any output on these cycles (see Figure 3).
DEAC, DCAB	The DQ bus is in the high-impedance state when n_{HZP} cycles are satisfied or when the read burst completes, whichever occurs first (see Figure 4).



NOTE A: For this example, assume read latency = 3 and burst length = 4.

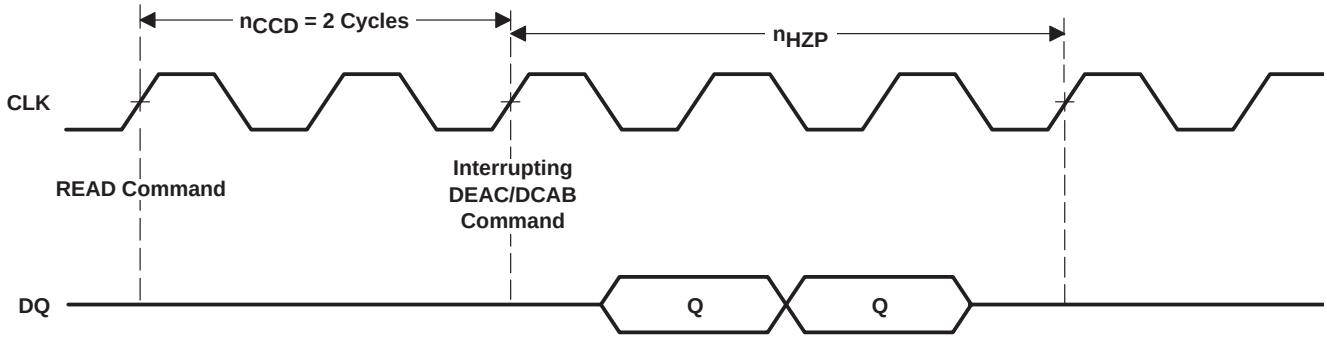
Figure 2. Read Burst Interrupted by Read Command

interrupted bursts (continued)



NOTES: A. For this example, assume read latency = 3 and burst length = 4.
B. DQMx must be high to mask output of the read burst on cycles (n_{CCD} – 1), n_{CCD}, and (n_{CDD} + 1).

Figure 3. Read Burst Interrupted by Write Command



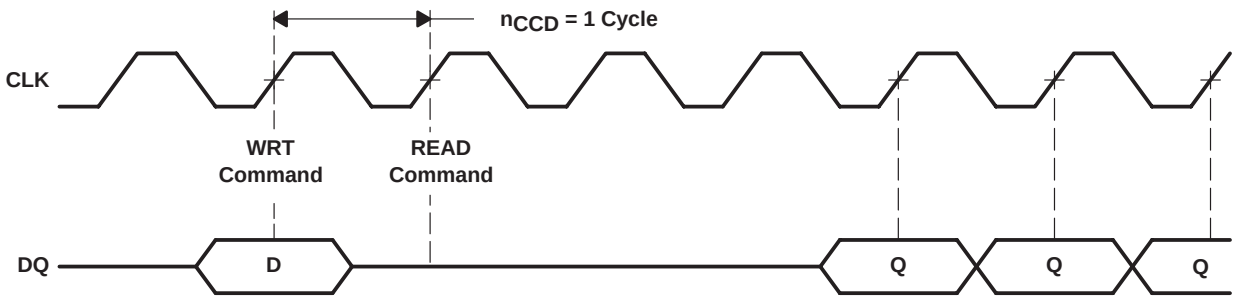
NOTE A: For this example, assume read latency = 3 and burst length = 4.

Figure 4. Read Burst Interrupted by DEAC Command

Table 8. Write-Burst Interruption

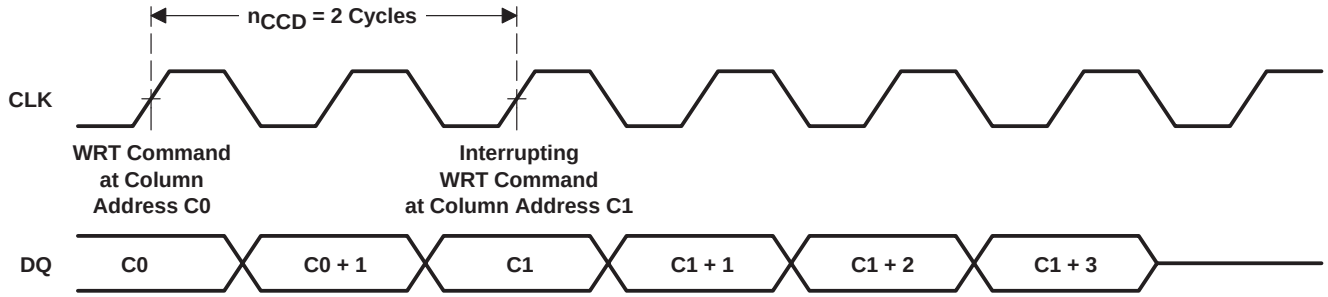
INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
READ, READ-P	Data that was input on the previous cycle is written; no further data inputs are accepted (see Figure 5).
WRT, WRT-P	The new WRT (WRT-P) command and data inputs immediately supersede the write burst in progress (see Figure 6).
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. DQMx must be used to mask the DQ bus such that the write recovery specification (t_{RWL}) is not violated by the interrupt (see Figure 7).

interrupted bursts (continued)



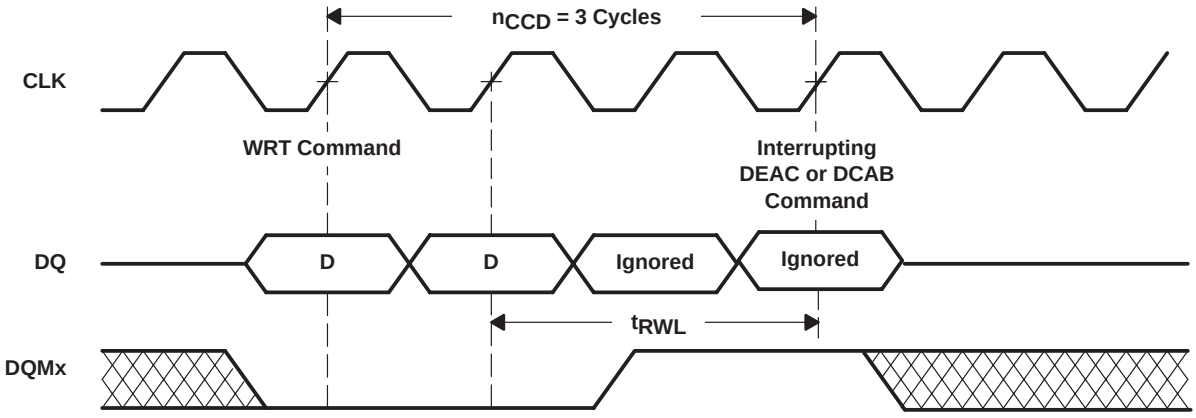
NOTE A: For this example, assume read latency = 3 and burst length = 4.

Figure 5. Write Burst Interrupted by Read Command



NOTE A: For this example, assume burst length = 4.

Figure 6. Write Burst Interrupted by Write Command



NOTE A: For this example, assume burst length = 4.

Figure 7. Write Burst Interrupted by DEAC/DCAB Command

power up

Device initialization should be performed after a power up to the full V_{CC} level; however, after power is established, a 200-µs interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands must be performed and the mode register must be set to complete the device initialization.

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 4.6 V
Supply voltage range for output drivers, V_{CCQ} . . . . . – 0.5 V to 4.6 V
Voltage range on any input pin (see Note 1) . . . . . – 0.5 V to 4.6 V
Voltage range on any output pin . . . . . – 0.5 V to V_{CC} + 0.5 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Ambient temperature range, T_A . . . . . – 55°C to 125°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.135	3.3	3.465	V
V_{CCQ}	Supply voltage for output drivers‡	3.135	3.3	3.465	V
V_{SS}	Supply voltage		0		V
V_{SSQ}	Supply voltage for output drivers		0		V
V_{IH}	High-level input voltage	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	– 0.3		0.8	V
T_A	Ambient temperature	–55		125	°C

‡ $V_{CCQ} \leq V_{CC}$ + 0.3 V

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		'626162-12		'626162-15		'626162-20		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –2 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	0 V ≤ V_I ≤ V_{CC}, All other pins = 0 V to V_{CC}			±10		±10		±10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CCQ}, Output disabled			±10		±10		±10	µA
I_{CC1}	Average read or write current	Burst length = 1, t_{RC} ≥ t_{RC} MIN, I_{OH}/I_{OL} = 0 mA, One bank activated (see Note 3)	Read latency = 2		85		75		70	mA
			Read latency = 3		100		95		85	
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = MIN (see Note 4)			2		2		2	mA
I_{CC2PS}		CKE and CLK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 5)			2		2		2	
I_{CC2N}	Precharge standby current in nonpower-down mode	CKE ≥ V_{IH} MIN, t_{CK} = MIN (see Note 4)			40		35		30	mA
I_{CC2NS}		CKE ≥ V_{IH} MIN, CLK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 5)			2		2		2	
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = MIN One bank activated (see Note 4)			10		10		10	mA
I_{CC3PS}		CKE and CLK ≤ V_{IL} MAX, t_{CK} = ∞ One bank activated (see Note 5)			10		10		10	
I_{CC3N}	Active standby current in nonpower-down mode	CKE ≥ V_{IH} MIN, t_{CK} = MIN One bank activated (see Note 4)			55		45		40	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CLK ≤ V_{IL} MAX, t_{CK} = ∞, One bank activated (see Note 5)			15		15		15	
I_{CC4}	Burst current	Continuous burst, I_{OH}/I_{OL} = 0 mA, All banks activated, n_{CCD} = one cycle (see Note 6)	Read latency = 2		165		130		110	mA
			Read latency = 3		210		175		150	
I_{CC5}	Autorefresh	t_{RC} ≥ t_{RC} MIN	Read latency = 2		120		100		80	mA
			Read latency = 3		120		100		80	

NOTES: 2. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
3. Control and address inputs change state twice during t_{RC}.
4. Control and address inputs change state once every 2 × t_{CK}.
5. Control and address inputs do not change state (stable).
6. Control and address inputs change state once every cycle.

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 7)

PARAMETER		MIN	MAX	UNIT
$C_{i(S)}$	Input capacitance, CLK input		8	pF
$C_{i(AC)}$	Input capacitance, address and control inputs: A0–A11, $\overline{CS}$, DQMx, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		8	pF
$C_{i(E)}$	Input capacitance, CKE input		8	pF
C_o	Output capacitance		10	pF

NOTE 7: Capacitance is sampled only at initial design and after any major changes. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the pin under test. All other pins are open.

ac timing requirements†‡

			'626162-12		'626162-15		'626162-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CK}	Cycle time, CLK (system clock)	Read latency = 2	15		20		30		ns
		Read latency = 3	12		15		20		
t_{CKH}	Pulse duration, CLK (system clock) high		4		4		4		ns
t_{CKL}	Pulse duration, CLK (system clock) low		4		4		4		ns
t_{AC}	Access time, CLK ↑ to data out (see Note 8)	Read latency = 2		9		15		20	ns
		Read latency = 3		8		9		10	
t_{LZ}	Delay time, CLK to DQ in the low-impedance state (see Note 9)		0		0		0		ns
t_{HZ}	Delay time, CLK to DQ in the high-impedance state (see Note 10)	Read latency = 2		8		14		15	ns
		Read latency = 3		8		11		12	
t_{DS}	Setup time, data input		3		4		4		ns
t_{AS}	Setup time, address		3		4		4		ns
t_{CS}	Setup time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQMx)		3		4		4		ns
t_{CES}	Setup time, CKE (suspend entry/exit, power-down entry)		3		4		4		ns
t_{CESP}	Setup time, CKE (power-down/self-refresh exit) (see Note 11)		10		10		10		ns
t_{OH}	Hold time, CLK ↑ to data out		1.5		2		2		ns
t_{DH}	Hold time, data input		2		2		2		ns
t_{AH}	Hold time, address		2		2		2		ns
t_{CH}	Hold time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQMx)		2		2		2		ns
t_{CEH}	Hold time, CKE		2		2		2		ns
t_{RC}	REFR command to ACTV, MRS, or REFR command; ACTV command to ACTV, MRS, or REFR command		96		120		160		ns
t_{RAS}	ACTV command to DEAC or DCAB command		60	100 000	75	100 000	100	100 000	ns
t_{RCD}	ACTV command to READ or WRT command (see Note 12)		24		30		40		ns
t_{RP}	DEAC or DCAB command to ACTV, MRS, or REFR command		36		45		60		ns

† See Parameter Measurement Information for load circuits.
‡ All references are made to the rising transition of CLK unless otherwise noted.

NOTES: 8. t_{AC} is referenced from the rising transition of CLK that precedes the data-out cycle. For example, the first data-out t_{AC} is referenced from the rising transition of CLK that is one cycle before read latency for the READ command. Access time is measured at output reference level 1.4 V.
9. t_{LZ} is measured from the rising transition of CLK that is one cycle before read latency for the READ command.
10. t_{HZ} (MAX) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
11. See Figure 18.
12. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.

ac timing requirements†‡ (continued)

		’626162-12		’626162-15		’626162-20		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{APR}	Final data out of READ-P operation to ACTV, MRS, or REFR command	$t_{RP} + (n_{EP} \times t_{CK})$						ns
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, or REFR command	$t_{RP} + t_{CK}$						ns
t_{RWL}	Final data in to DEAC or DCAB command	24		30		40		ns
t_{RRD}	ACTV command for one bank to ACTV command for the other bank	24		30		40		ns
t_T	Transition time, all inputs (see Note 13)	1	5	1	5	1	5	ns
t_{REF}	Refresh interval		32		32		32	ms

† See Parameter Measurement Information for load circuits.
‡ All references are made to the rising transition of CLK unless otherwise noted.
NOTE 13: Transition time (rise and fall) should be a minimum of 1 ns and a maximum of 5 ns measured between V_{IH} MIN and V_{IL} MAX. This is ensured by design but not tested.

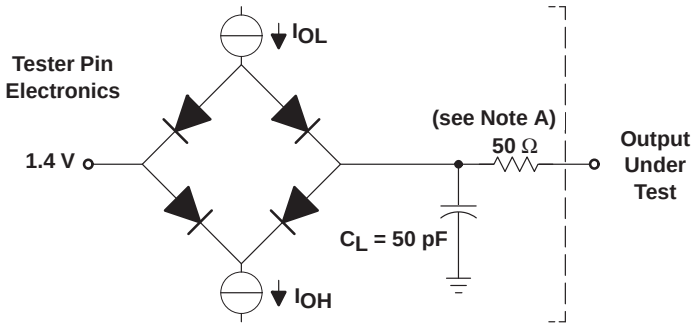
clock timing requirements‡§

			’626162-12		’626162-15		’626162-20		UNIT§
			MIN	MAX	MIN	MAX	MIN	MAX	
n_{EP}	Final data out to DEAC or DCAB command	Read latency = 2	–1		–1		–1		cycles
		Read latency = 3	–2		–2		–2		
n_{HZP}	DEAC or DCAB interrupt of data-out burst to DQ in the high-impedance state	Read latency = 2	2		2		2		cycles
		Read latency = 3	3		3		3		
n_{CCD}	READ or WRT command to interrupting READ, WRT, DEAC, or DCAB command		1		1		1		cycles
n_{CWL}	Final data in to READ or WRT command in either bank		1		1		1		cycles
n_{WCD}	WRT command to first data in		0	0	0	0	0	0	cycles
n_{DID}	ENBL or MASK command to data in		0	0	0	0	0	0	cycles
n_{DOD}	ENBL or MASK command to data out		2	2	2	2	2	2	cycles
n_{CLE}	HOLD command to suspended CLK edge; HOLD operation exit to entry of any command		1	1	1	1	1	1	cycles
n_{RSA}	MRS command to ACTV, REFR, or MRS command		2		2		2		cycles
n_{CDD}	DESL command to control input inhibit		0	0	0	0	0	0	cycles

‡ All references are made to the rising transition of CLK unless otherwise noted.
§ A CLK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CLK cycles occurring during the time when CKE is asserted low).

PARAMETER MEASUREMENT INFORMATION

The ac timing measurements are based on signal rise and fall times equal to 1 ns (t_T = 1 ns) and a midpoint reference level of 1.4 V for LVTTL. For signal rise and fall times greater than 1 ns, the reference level is changed to V_{IH} MIN and V_{IL} MAX instead of the midpoint level. All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted. All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted. All specifications referring to consecutive commands are specified as consecutive commands for the same bank unless otherwise noted.



NOTE A: Series termination resistors may be used on test hardware for output impedance matching purposes.

Figure 8. LVTTL-Load Circuit

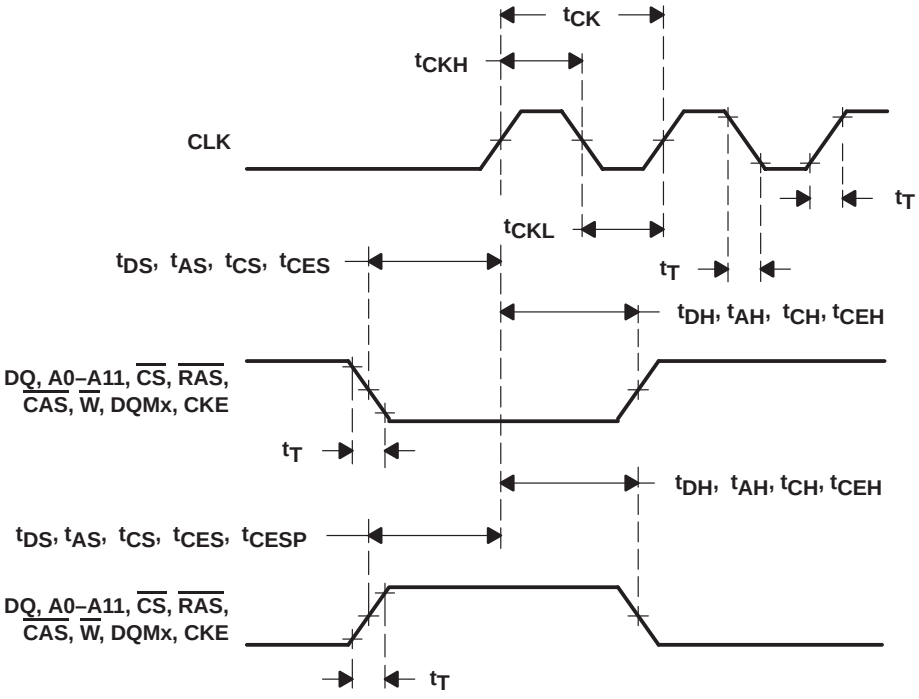


Figure 9. Input-Attribute Parameters

PARAMETER MEASUREMENT INFORMATION

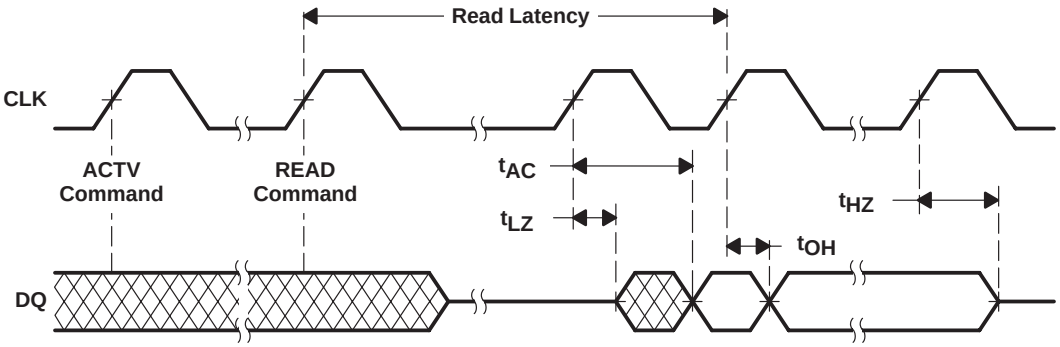


Figure 10. Output Parameters

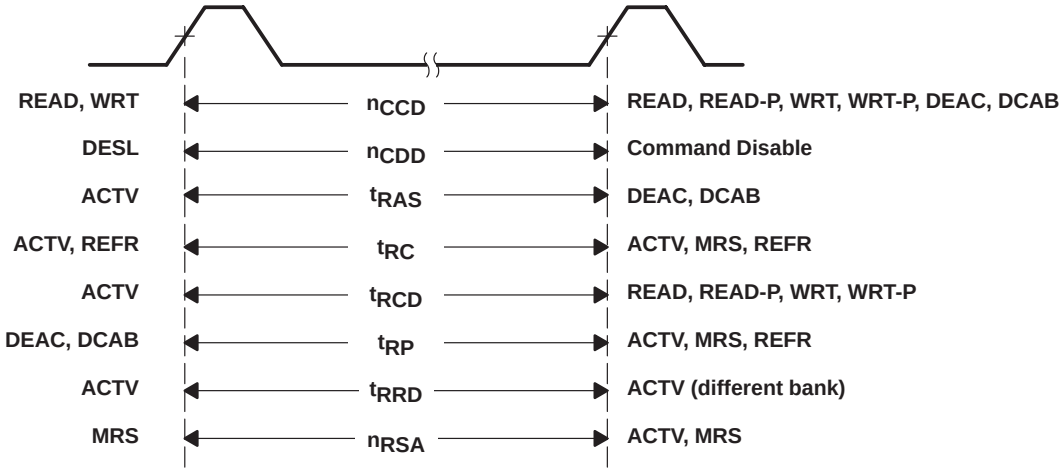
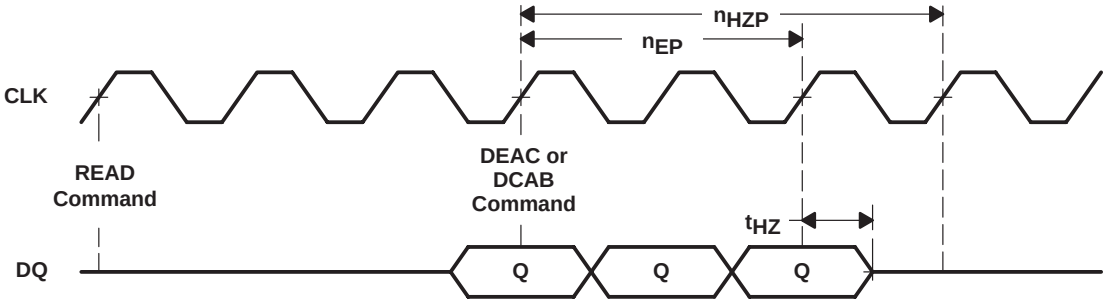


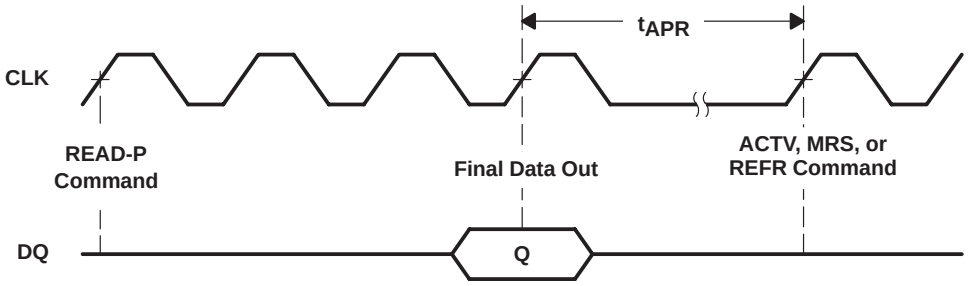
Figure 11. Command-to-Command Parameters

PARAMETER MEASUREMENT INFORMATION



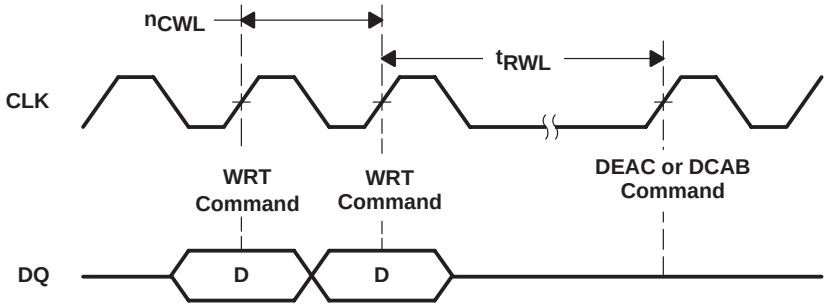
NOTE A: For this example, assume read latency = 3 and burst length = 4.

Figure 12. Read Followed by Deactivate



NOTE A: For this example, assume read latency = 3 and burst length = 1.

Figure 13. Read With Auto-Deactivate



NOTE A: For this example, assume burst length = 1.

Figure 14. Write Followed By Deactivate

PARAMETER MEASUREMENT INFORMATION

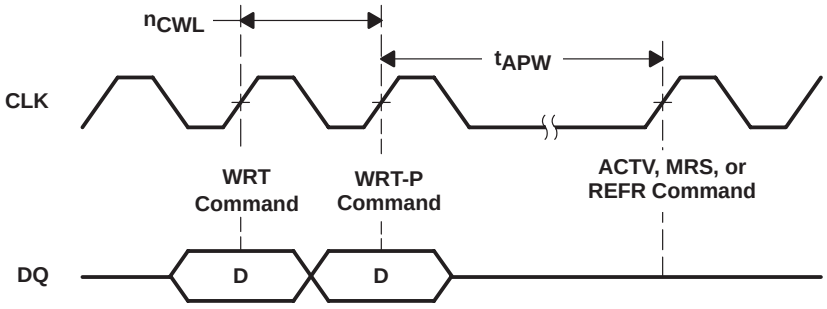
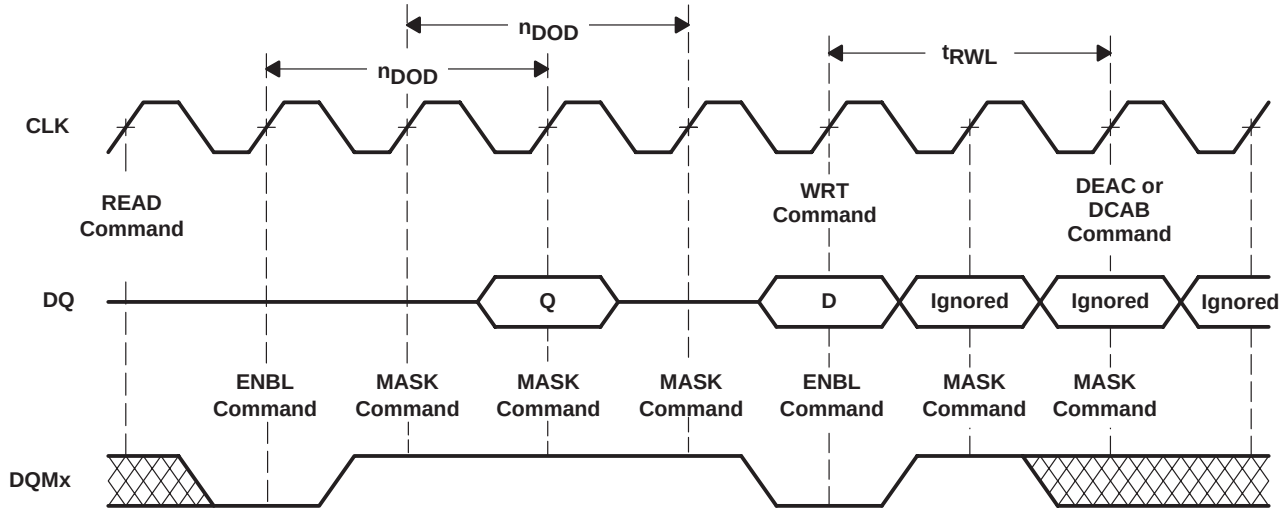


Figure 15. Write With Auto-Deactivate



NOTE A: For this example, assume read latency = 3 and burst length = 4.

Figure 16. DQ Masking

PARAMETER MEASUREMENT INFORMATION

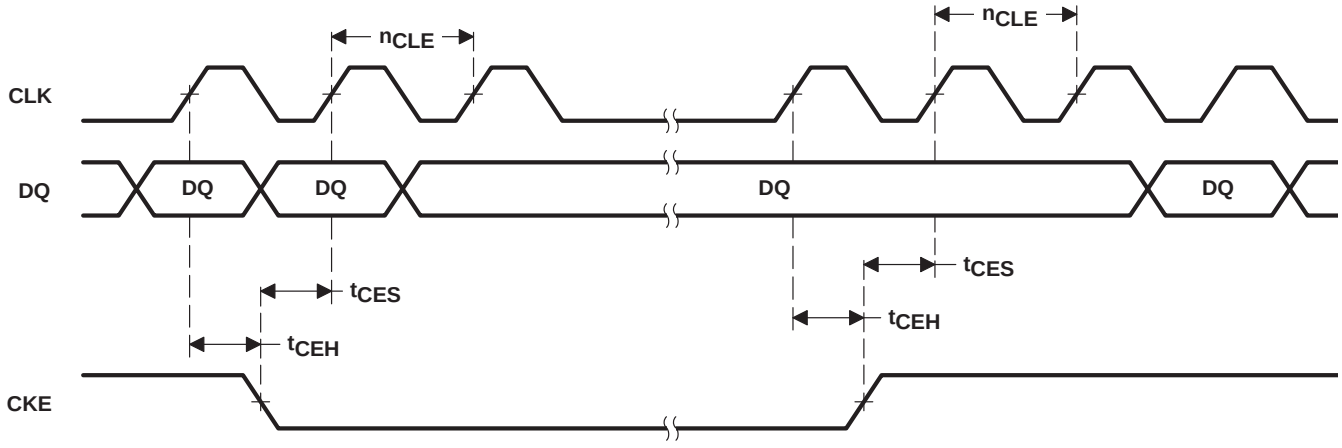


Figure 17. CLK-Suspend Operation

PARAMETER MEASUREMENT INFORMATION

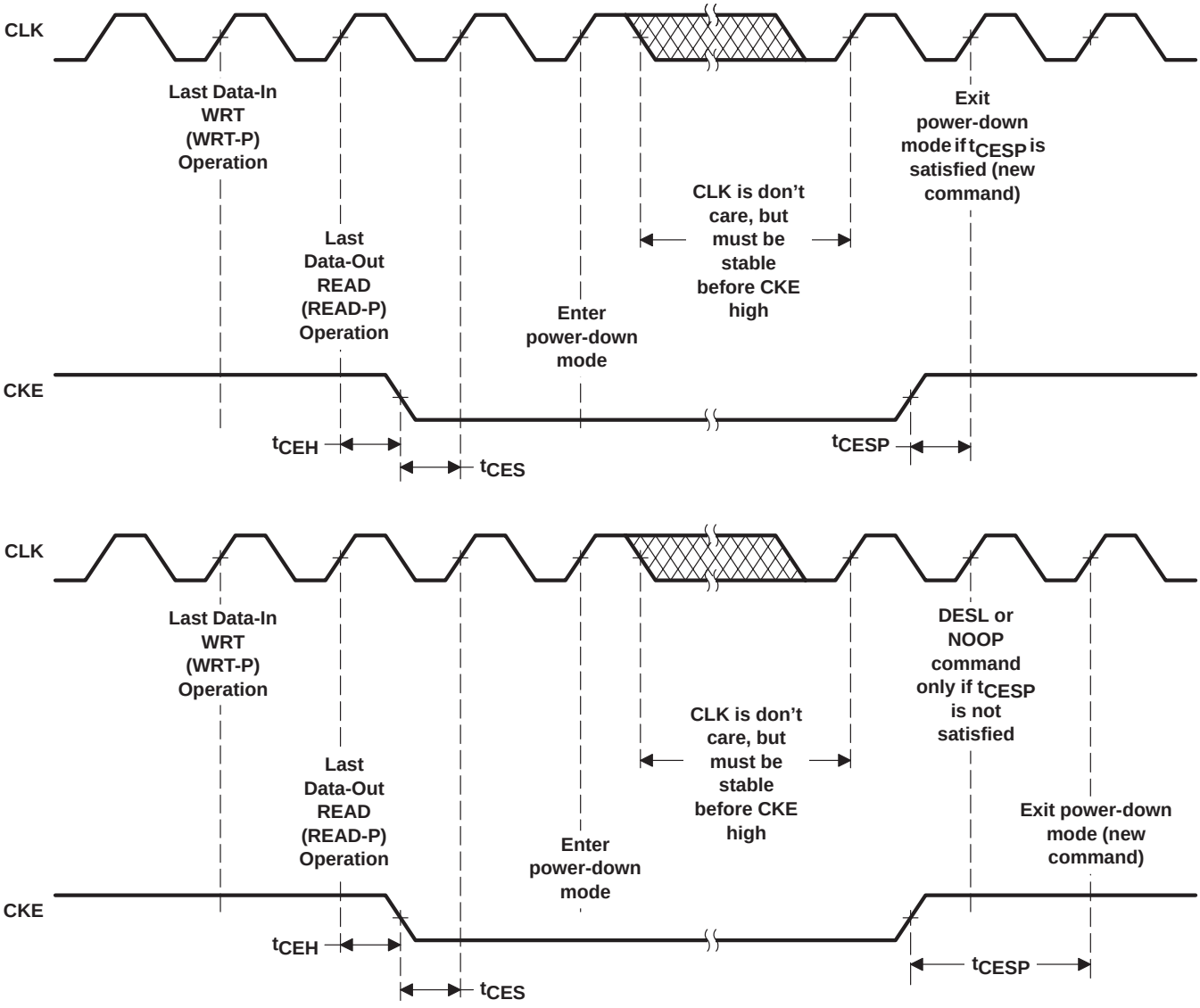
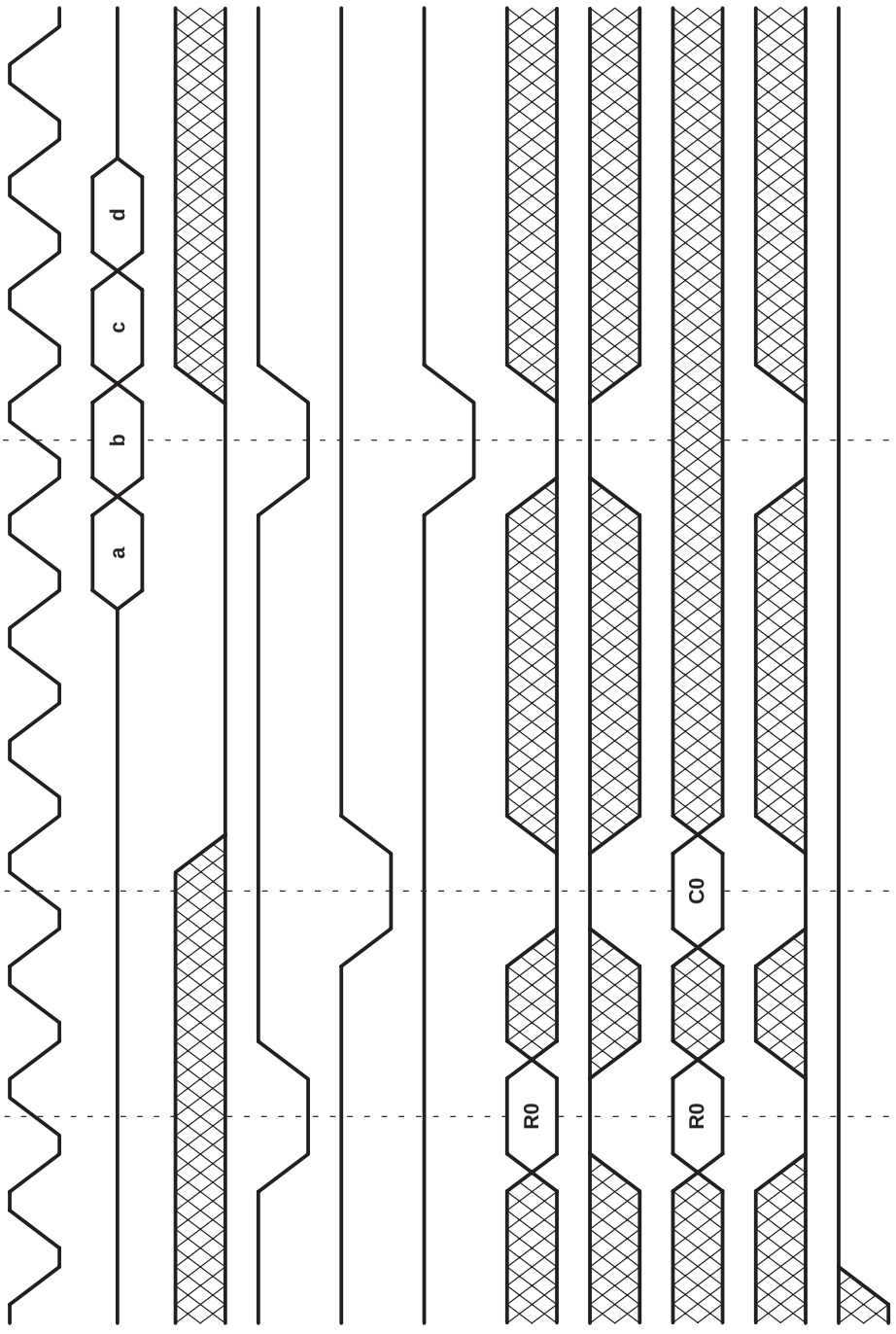


Figure 18. Power-Down Operation

PARAMETER MEASUREMENT INFORMATION



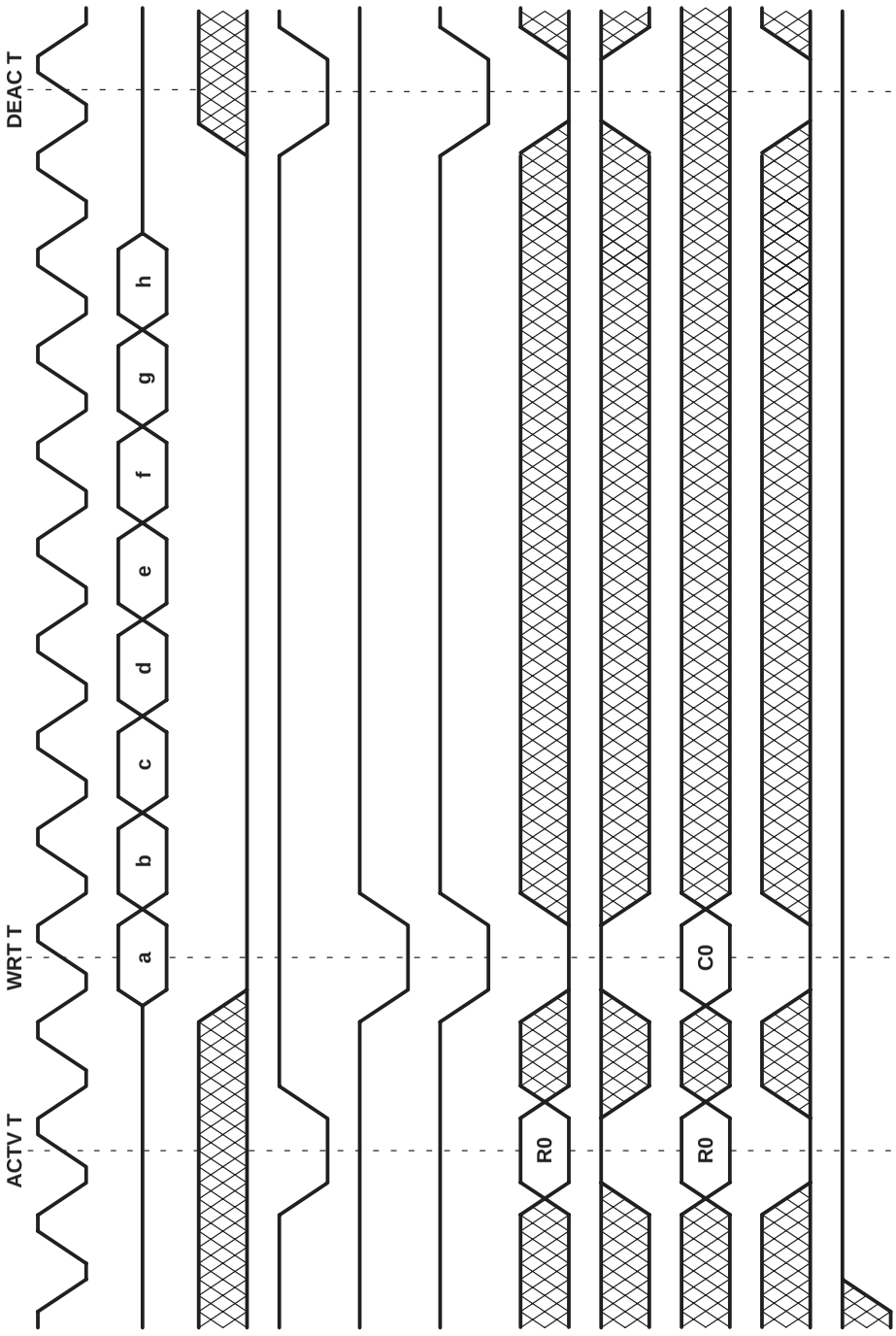
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5).

NOTE A: This example illustrates minimum t_{RCD} and n_{EP} for the '626162-15 at 66 MHz.

Figure 19. Read Burst (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



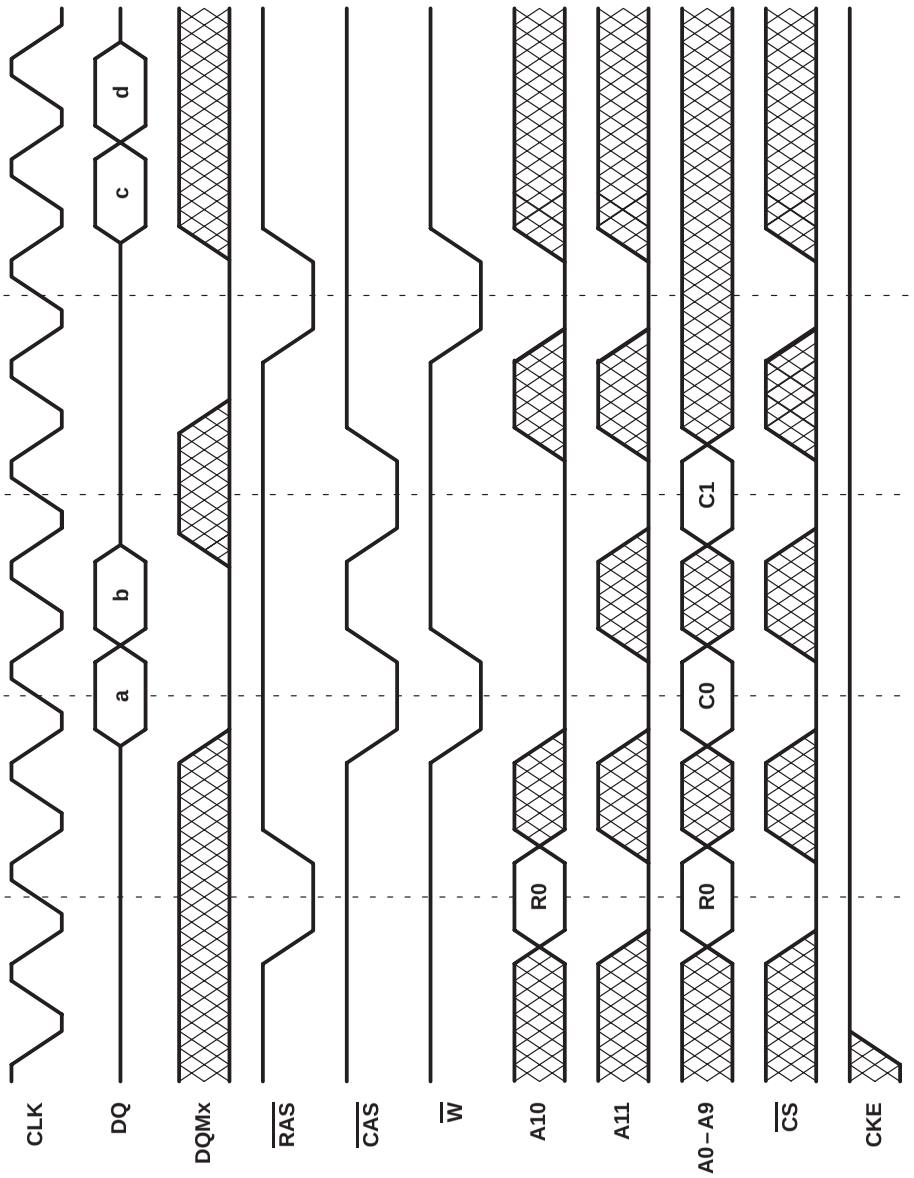
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
D	T	R0	C0	C0 + 1	C0 + 2	C0 + 3	C0 + 4	C0 + 5	C0 + 6	C0 + 7

† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} and t_{RWL} for the '626162-15 at 66 MHz.

Figure 20. Write Burst (burst length = 8)

PARAMETER MEASUREMENT INFORMATION



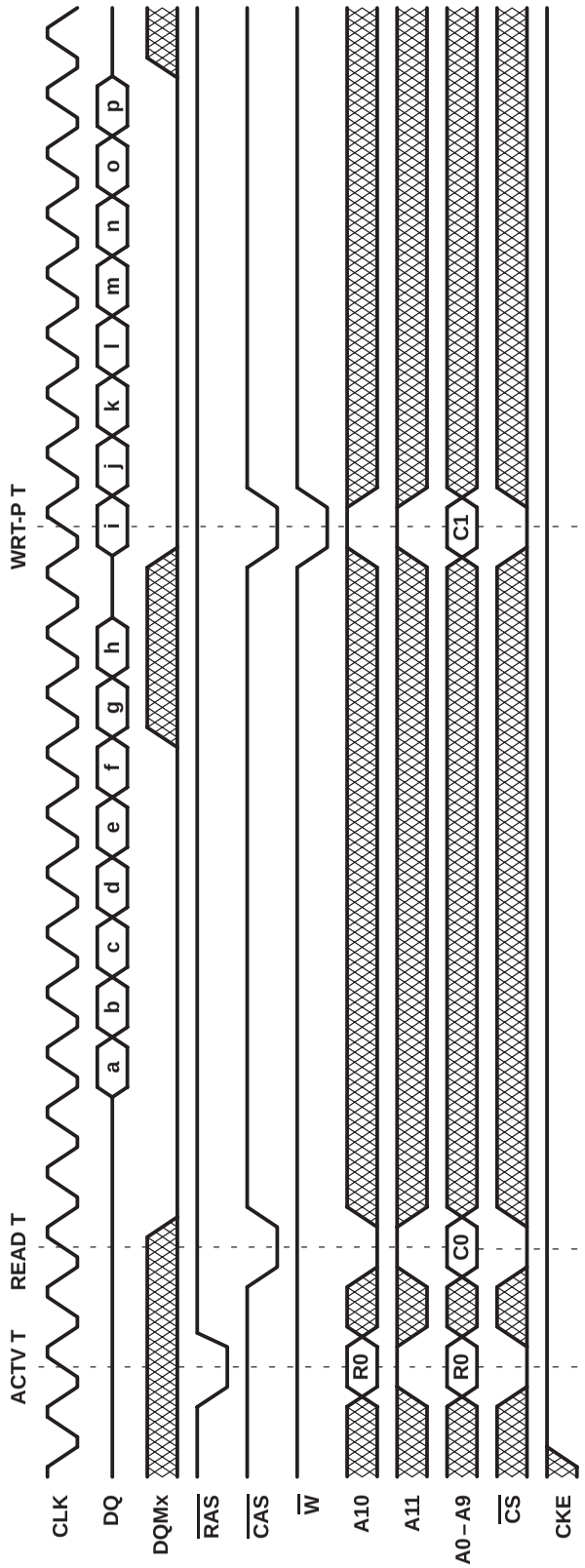
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
D	B	R0	C0	C0 + 1		
Q	B	R0			C1	C1 + 1

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 4).

NOTE A: This example illustrates minimum t_{RCD} and n_{EP} for the '626162-15 at 66 MHz.

Figure 21. Write-Read Burst (read latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION



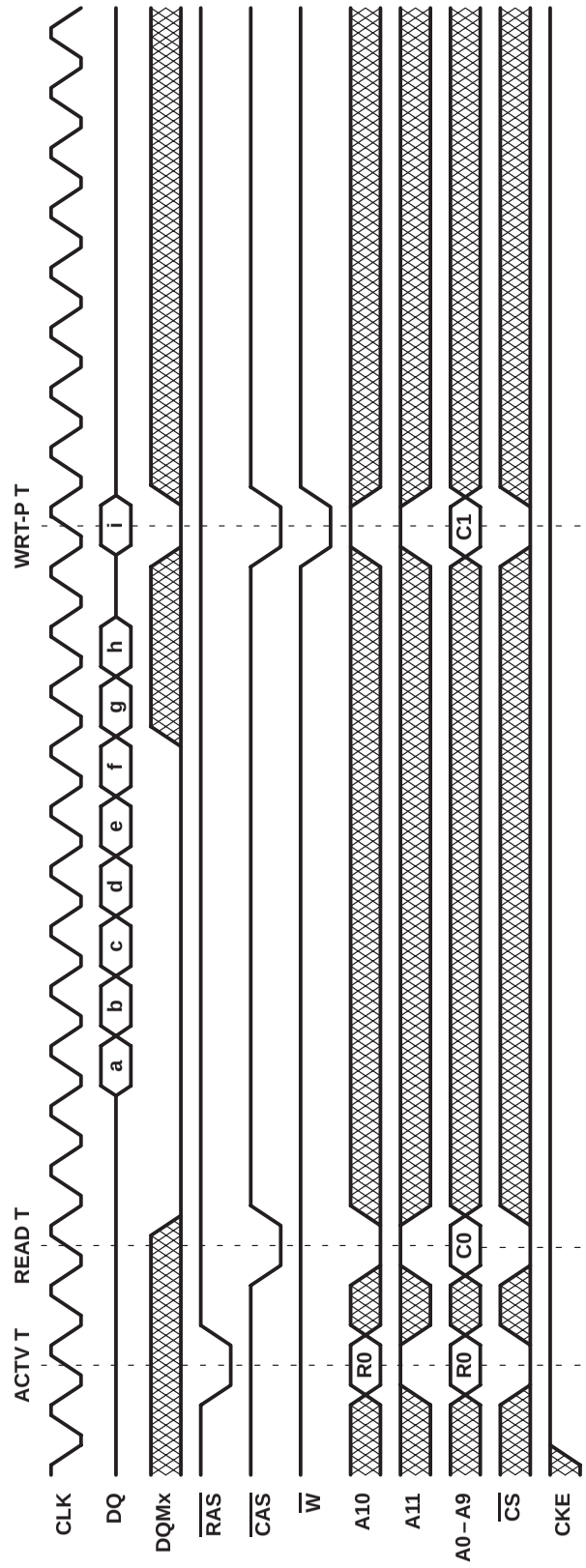
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
Q	T	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7								
D	T	R0									C1	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} for the '626162-15 at 66 MHz.

Figure 22. Read-Write Burst With Automatic Deactivate (read latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION



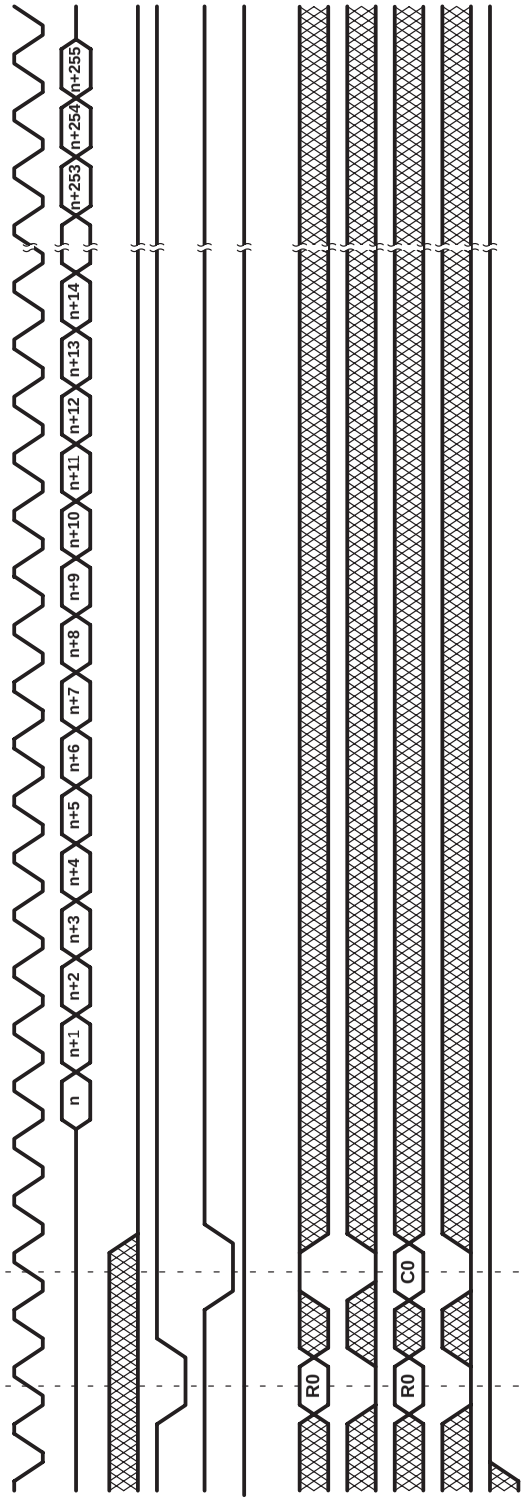
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h	i
Q	T	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7	
D	T	R0									C1

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} for the ‘626162-15 at 66 MHz.

Figure 23. Read Burst – Single Write With Automatic Deactivate (read latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION



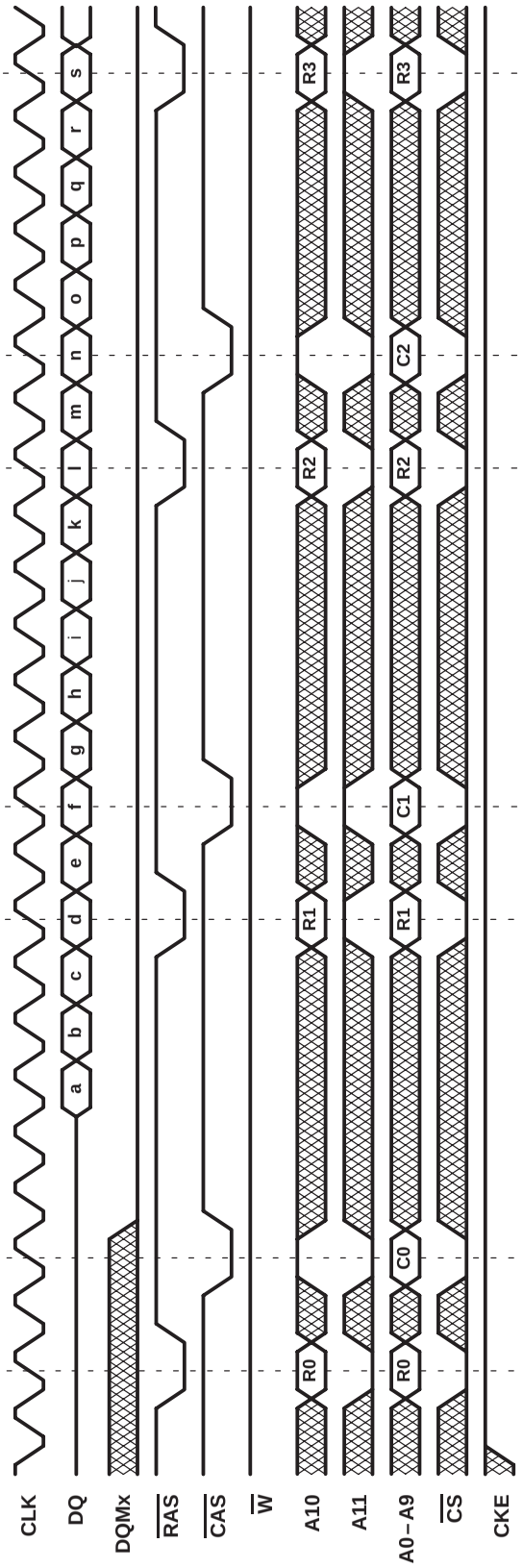
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	. . .	
Q	B	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7													255

† Column-address sequence depends on programmed burst type and starting column address C0.

NOTE A: This example illustrates minimum t_{RCD} for the '626162-15 at 66 MHz.

Figure 24. Read Burst – Full Page (read latency = 3, burst length = 256)

PARAMETER MEASUREMENT INFORMATION



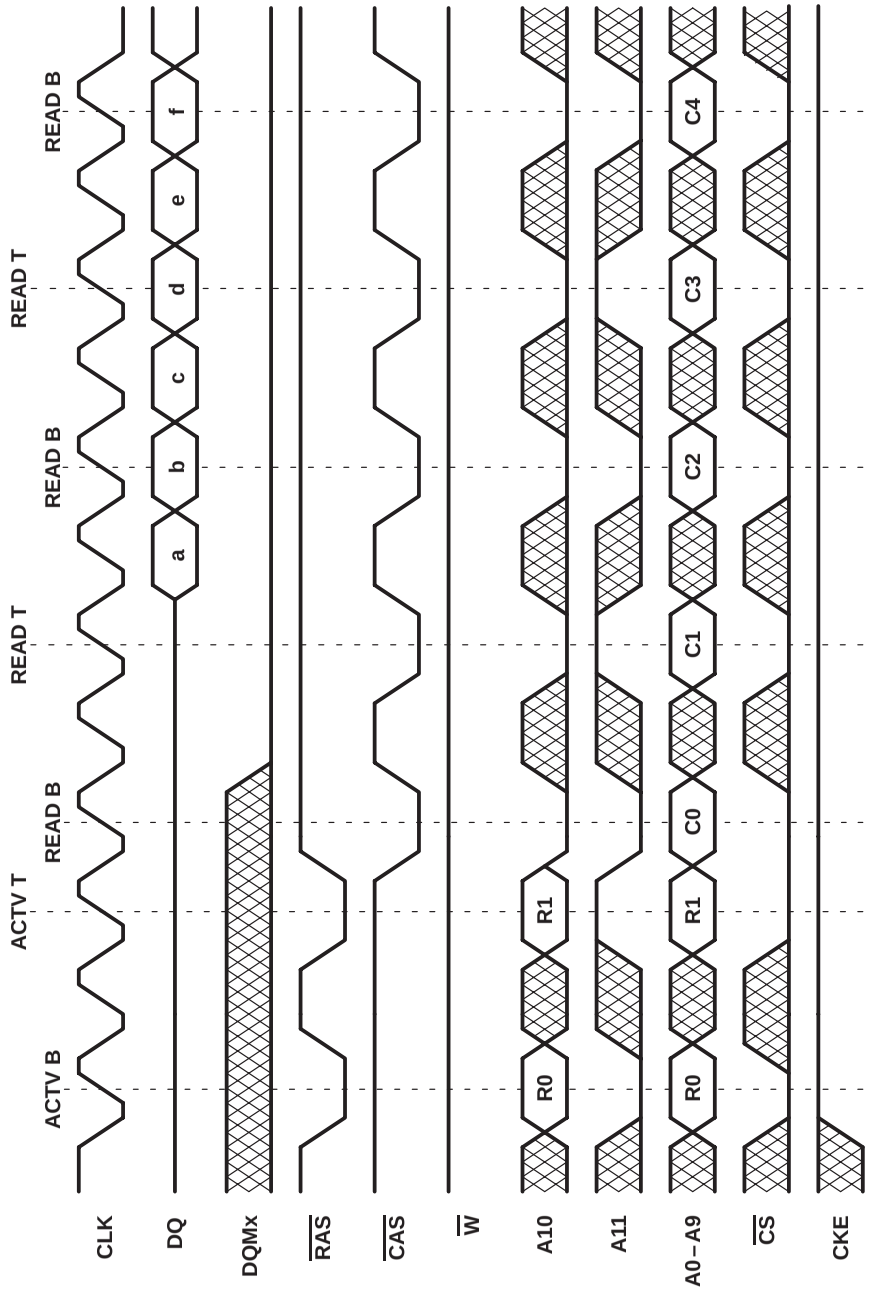
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	. . .
Q	B	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7												
Q	T	R1									C1	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7				
Q	B	R2																	C2	C2+1	C2+2	. . .

† Column-address sequence depends on programmed burst type and starting column address C0, C1, and C2 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} for the '626162-15 at 66 MHz.

Figure 25. Two-Bank Row-Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION

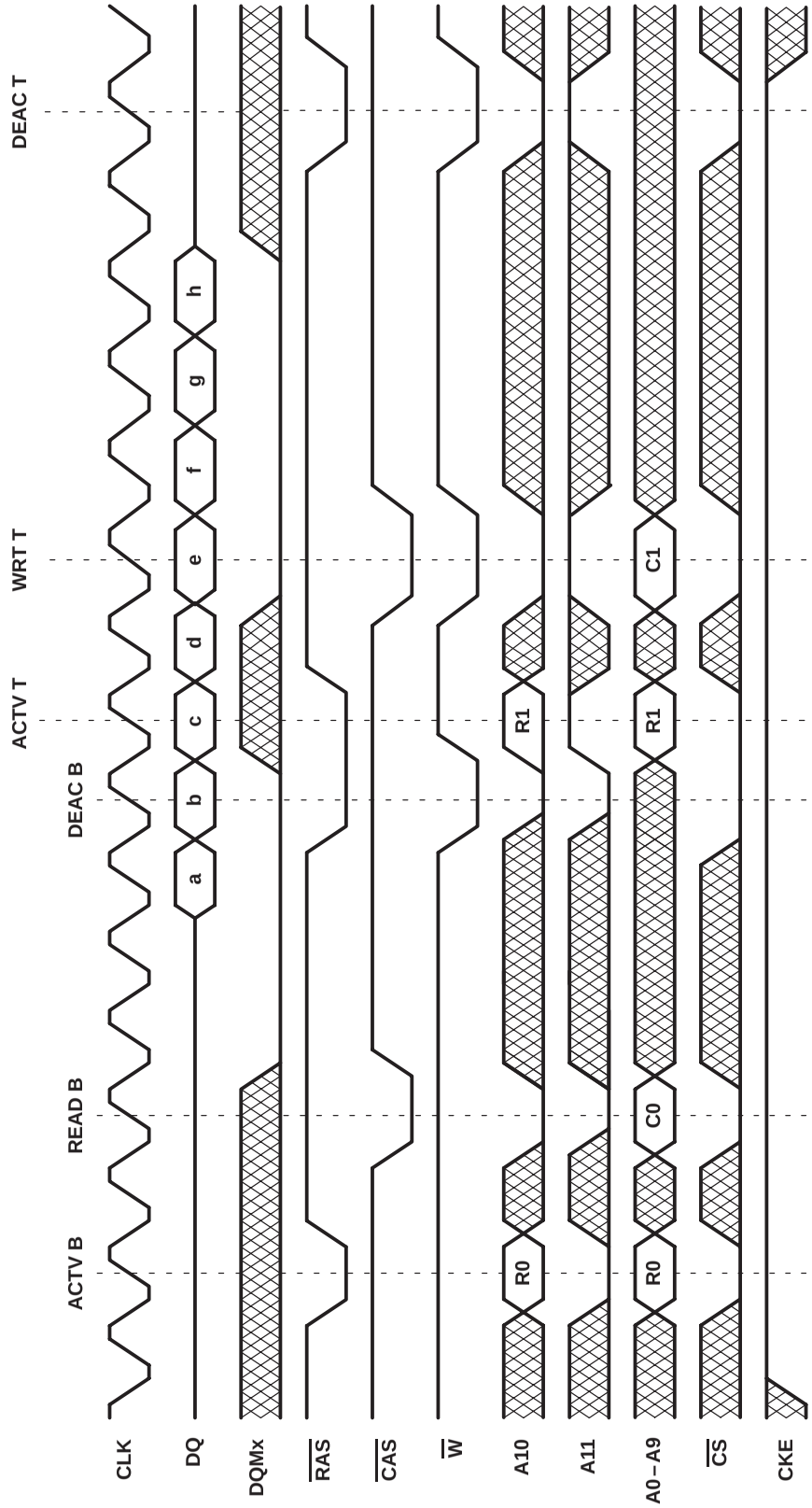


BURST TYPE	BANK	ROW	BURST CYCLE†							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	. . .	. . .
Q	B	R0	C0	C0 + 1	C1	C1 + 1	C2	C2 + 1	. . .	. . .
Q	T	R1								
Q	B	R0								
.	. . .	. . .								

† Column-address sequence depends on programmed burst type and starting column address C0, C1, and C2 (see Table 4).

Figure 26. Two-Bank Column-Interleaving Read Bursts (read latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION



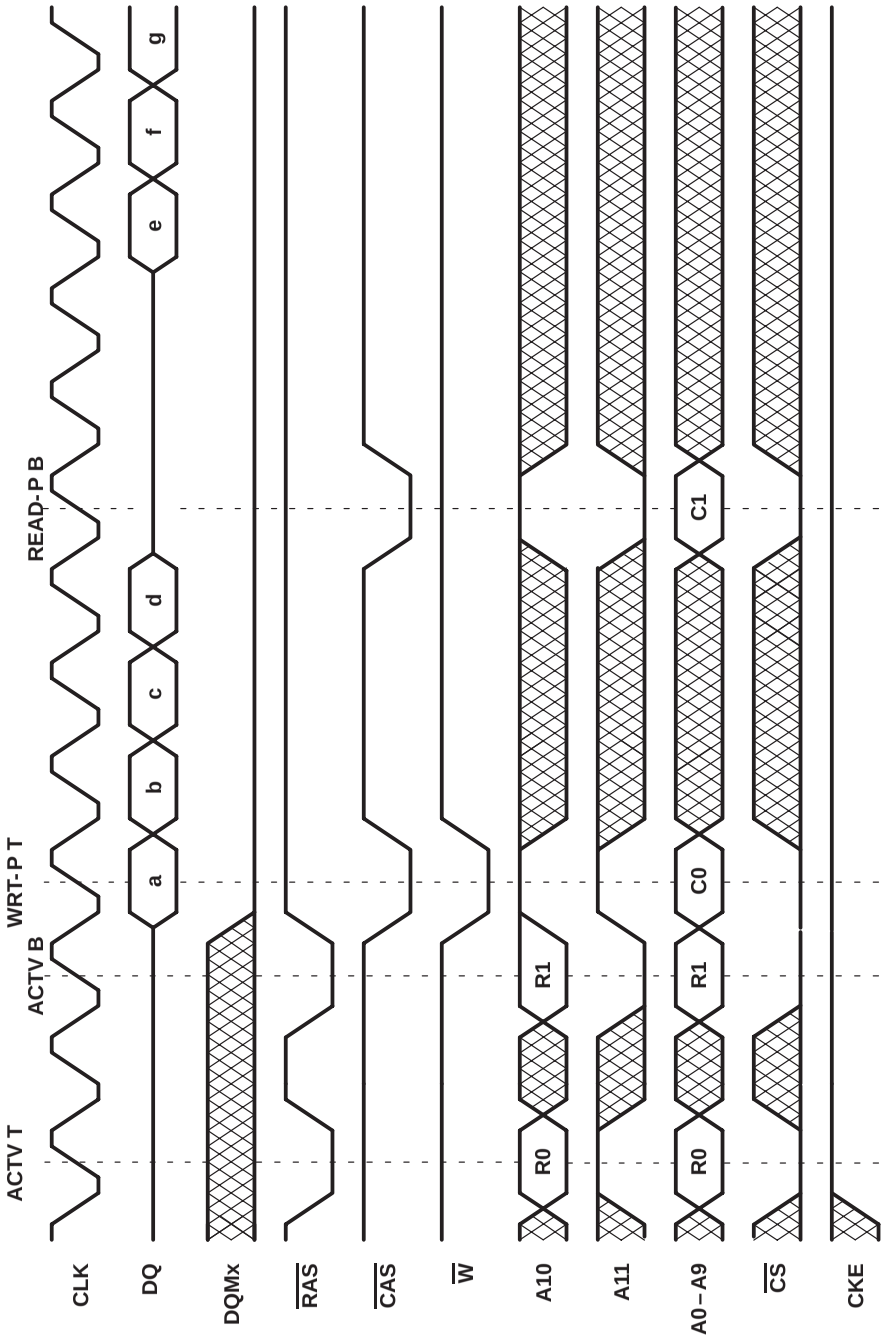
BURST TYPE	BANK	ROW	BURST CYCLE†							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	B	R0	C0	C0 + 1	C0 + 2	C0 + 3				
D	T	R1					C1	C1 + 1	C1 + 2	C1 + 3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5.)

NOTE A: This example illustrates minimum t_{RCD}, n_{EP}, and t_{RWL} for the '626162-15 at 66 MHz.

Figure 27. Read-Burst Bank B, Write-Burst Bank T (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



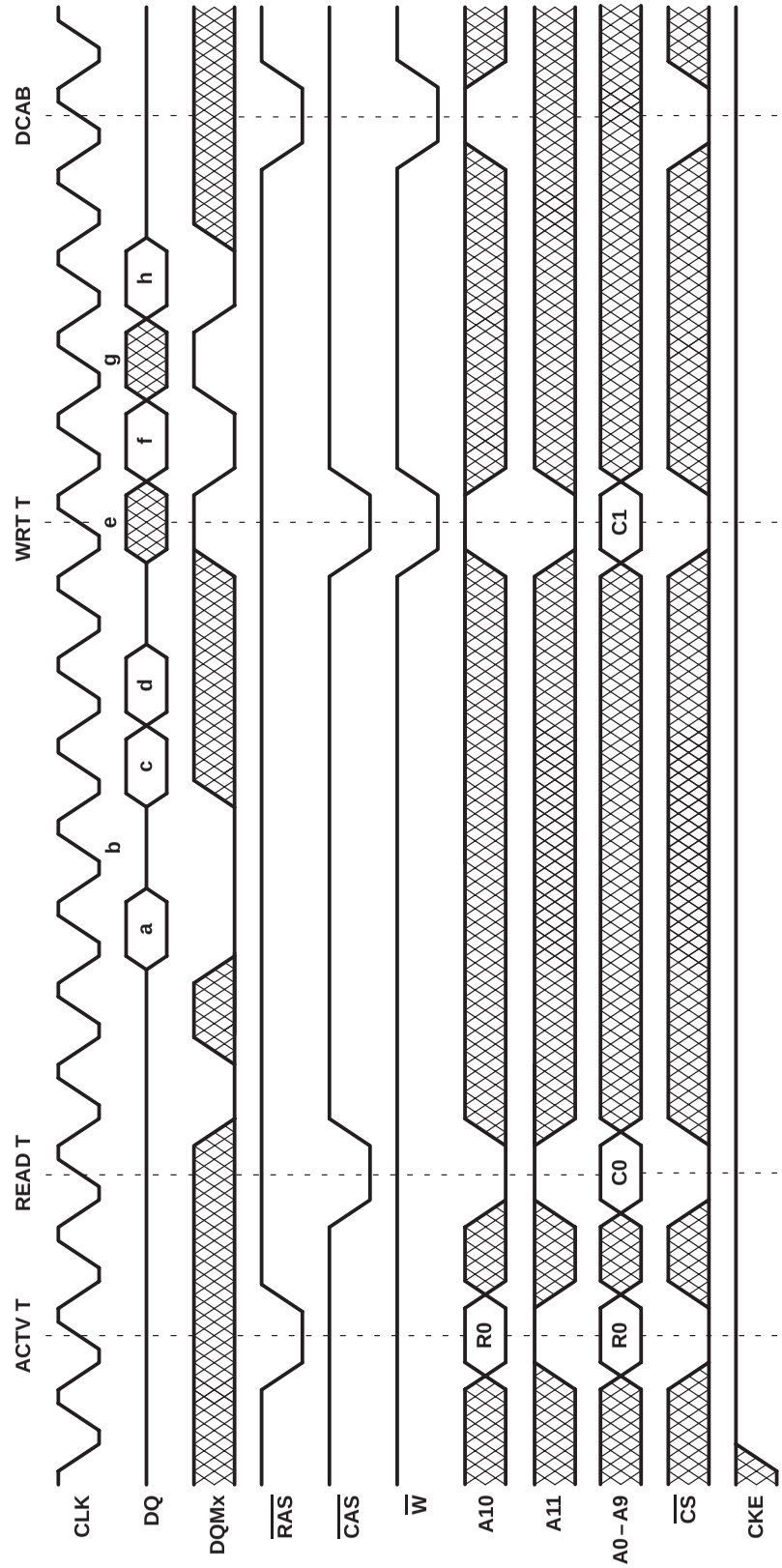
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
D	T	R0	C0	C0 + 1	C0 + 2	C0 + 3				
Q	B	R1					C1	C1 + 1	C1 + 2	C1 + 3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).

NOTE A: This example illustrates minimum n_{CWL} for the ’626162-15 at 66 MHz.

Figure 28. Write-Burst Bank T, Read-Burst Bank B With Automatic Deactivate (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



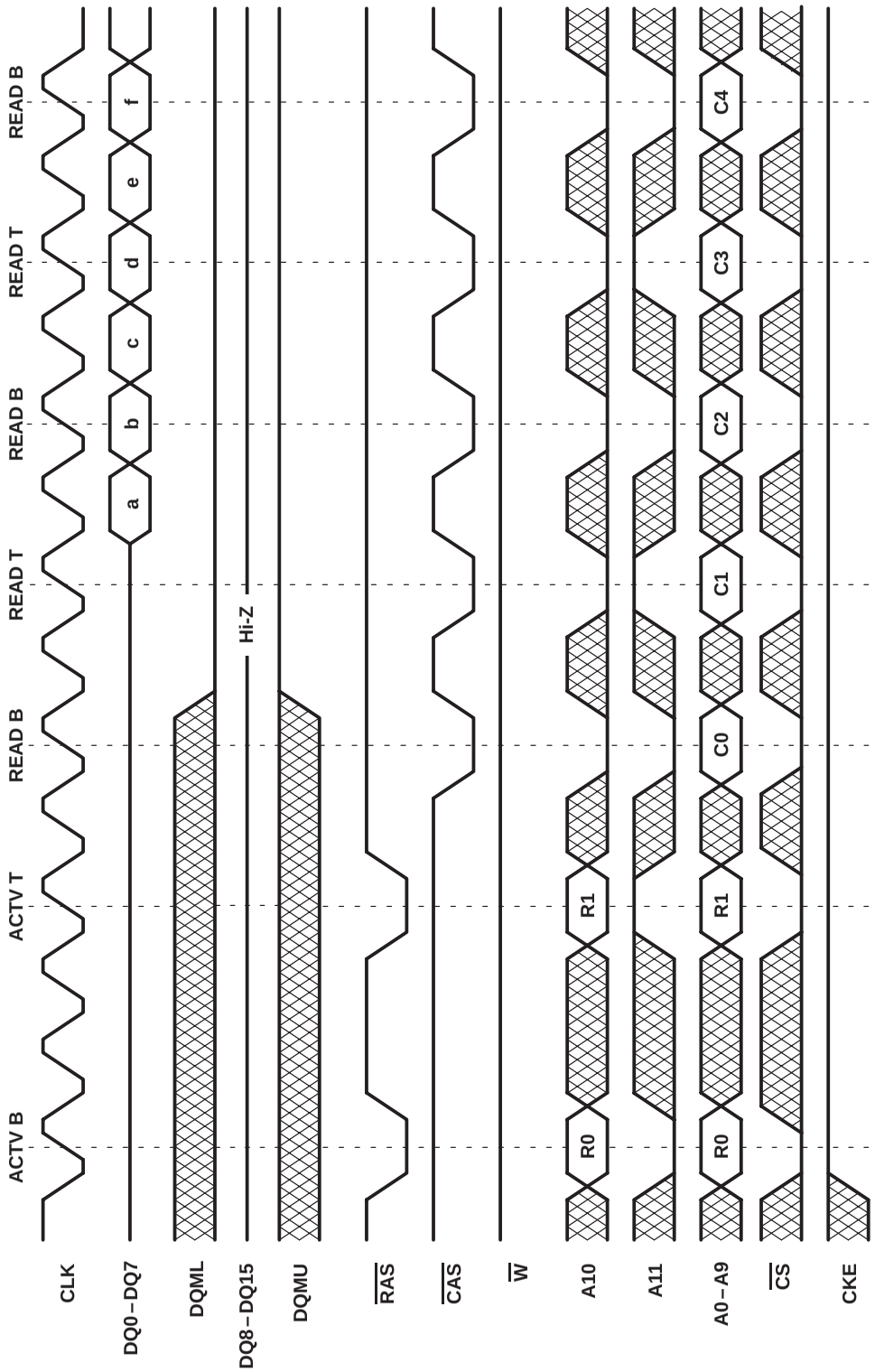
BURST TYPE	BANK	ROW	BURST CYCLE†							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1	C0+2	C0+3				
D	T	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).

NOTE A: This example illustrates minimum t_{RCD} for the '626162-15 at 66 MHz.

Figure 29. Data Mask (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

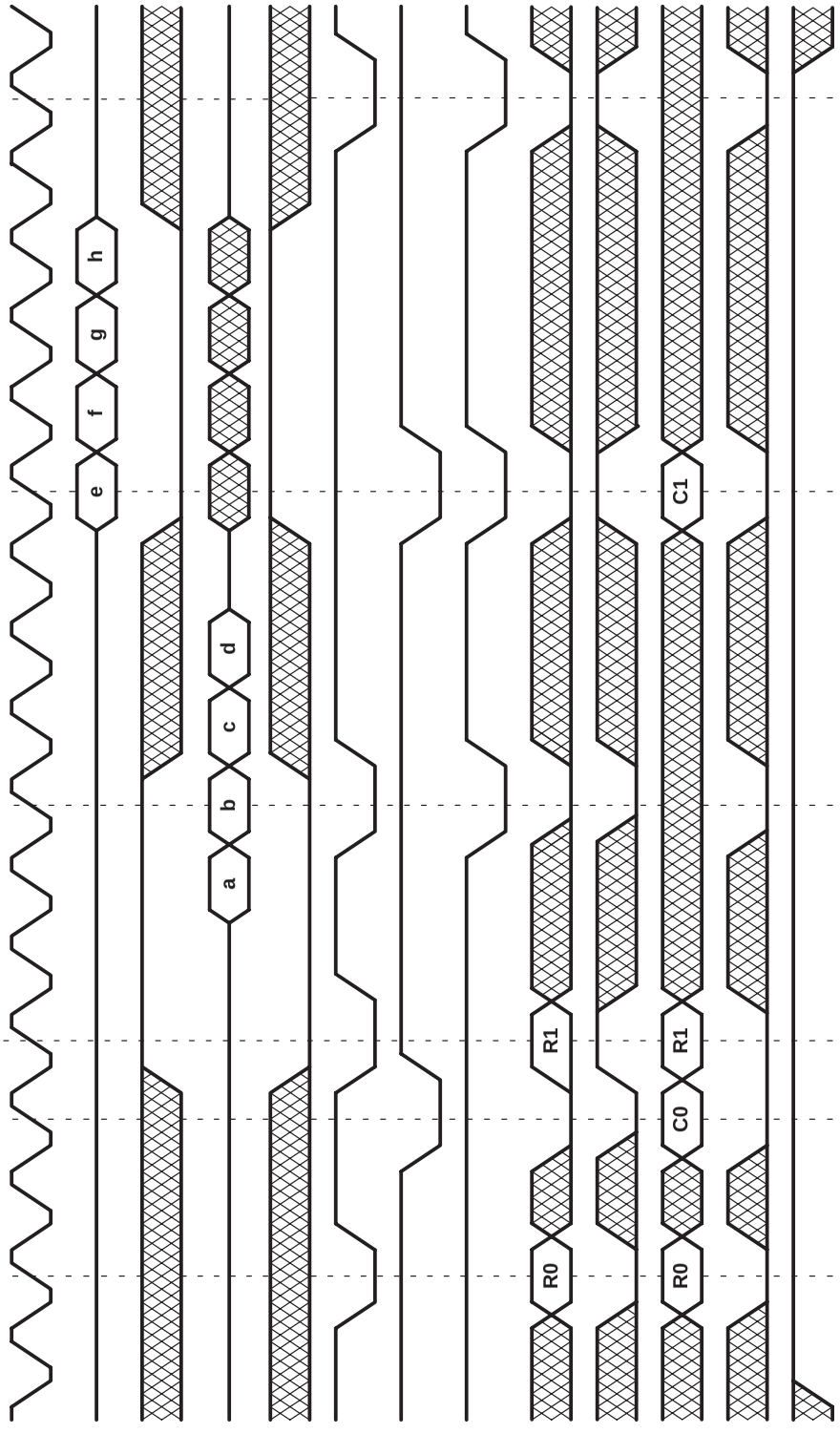


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1						
Q	B	R1			C1	C1+1				
Q	T	R0					C2	C1+1		
Q	B	R1							C3	C3+1

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 4).

Figure 30. Data Mask With Byte Control (read latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION



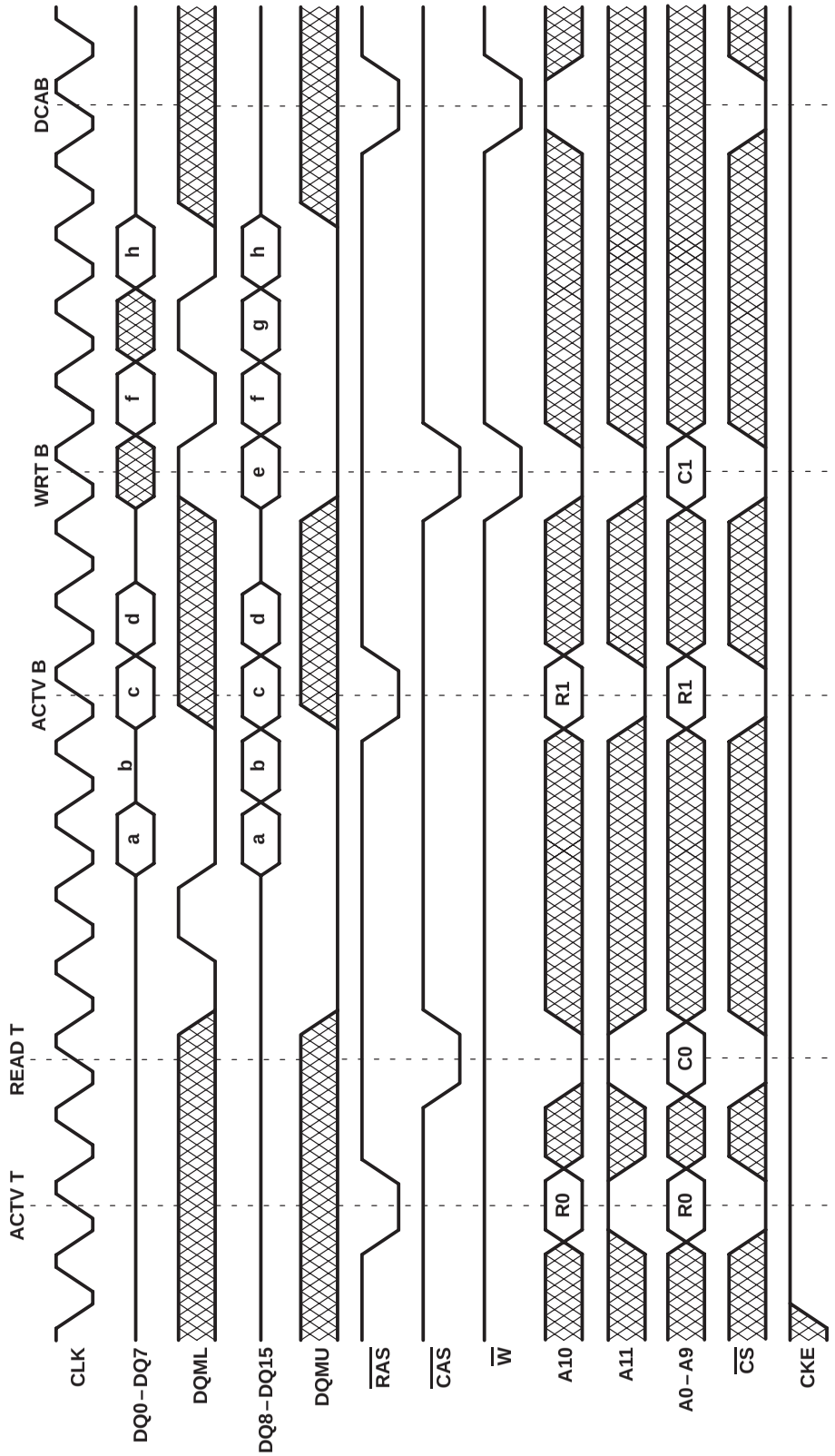
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1	C0+2	C0+3				
D	B	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).

NOTE A: This example illustrates minimum t_{RCD} and n_{EP} read burst, and a minimum t_{RWL} write burst for the '626162-15 at 66 MHz.

Figure 31. Data Mask With Byte Control (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

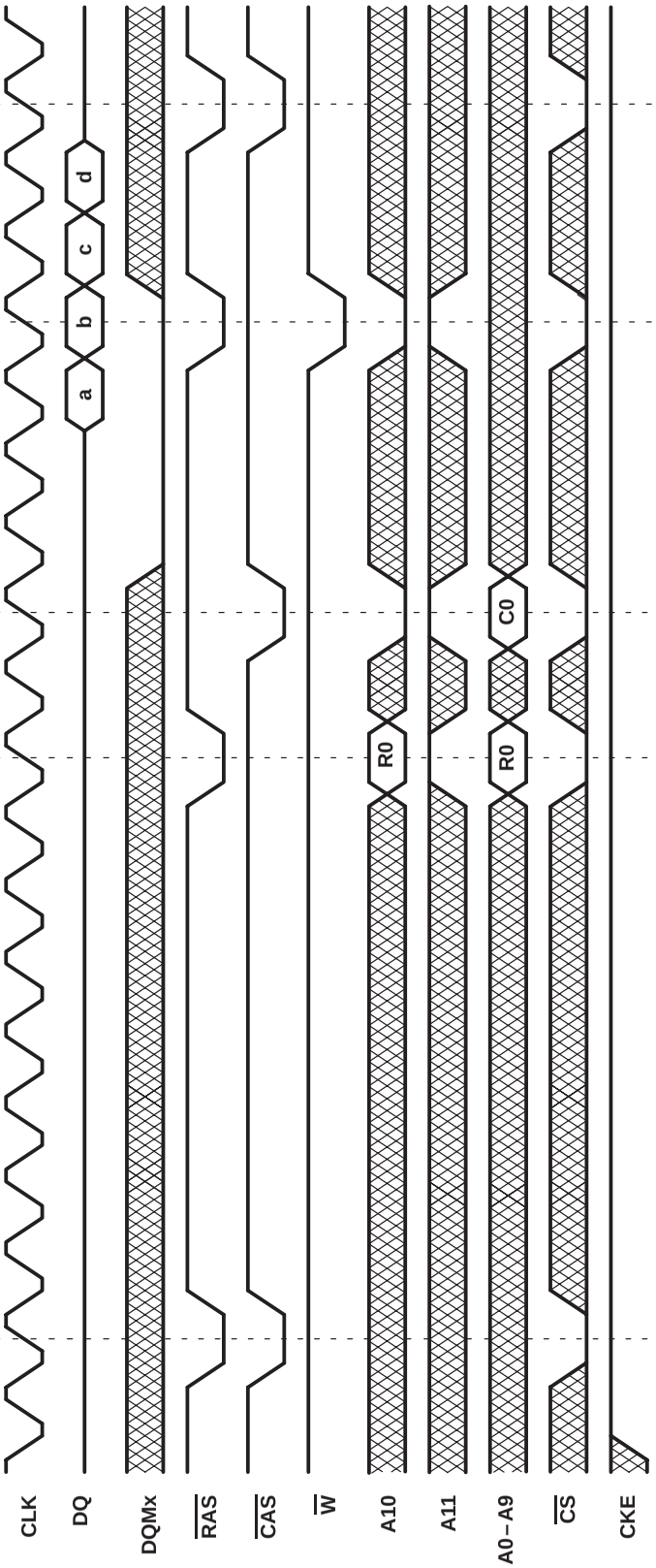


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1	C0+2	C0+3				
D	B	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} and t_{RWL} for the '626162-15 at 66 MHz.

Figure 32. Data Mask With Cycle-by-Cycle Byte Control (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



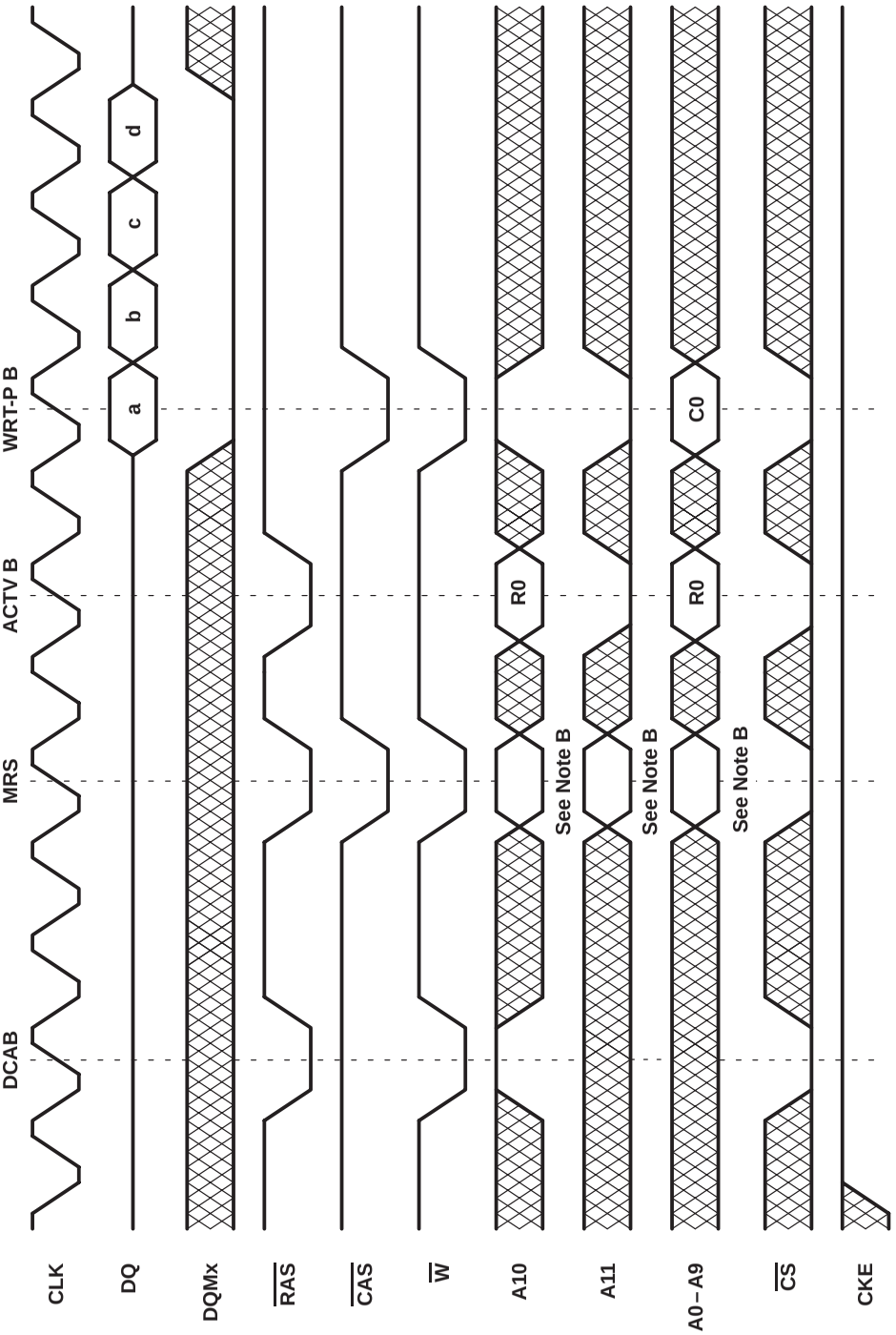
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
Q	T	R0	C0	C0+1	C0+2	C0+3

† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5).

NOTE A: This example illustrates minimuim t_{RC}, t_{RCD}, and n_{EP} for the '626162-15 at 66 MHz.

Figure 33. Refresh Cycles (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



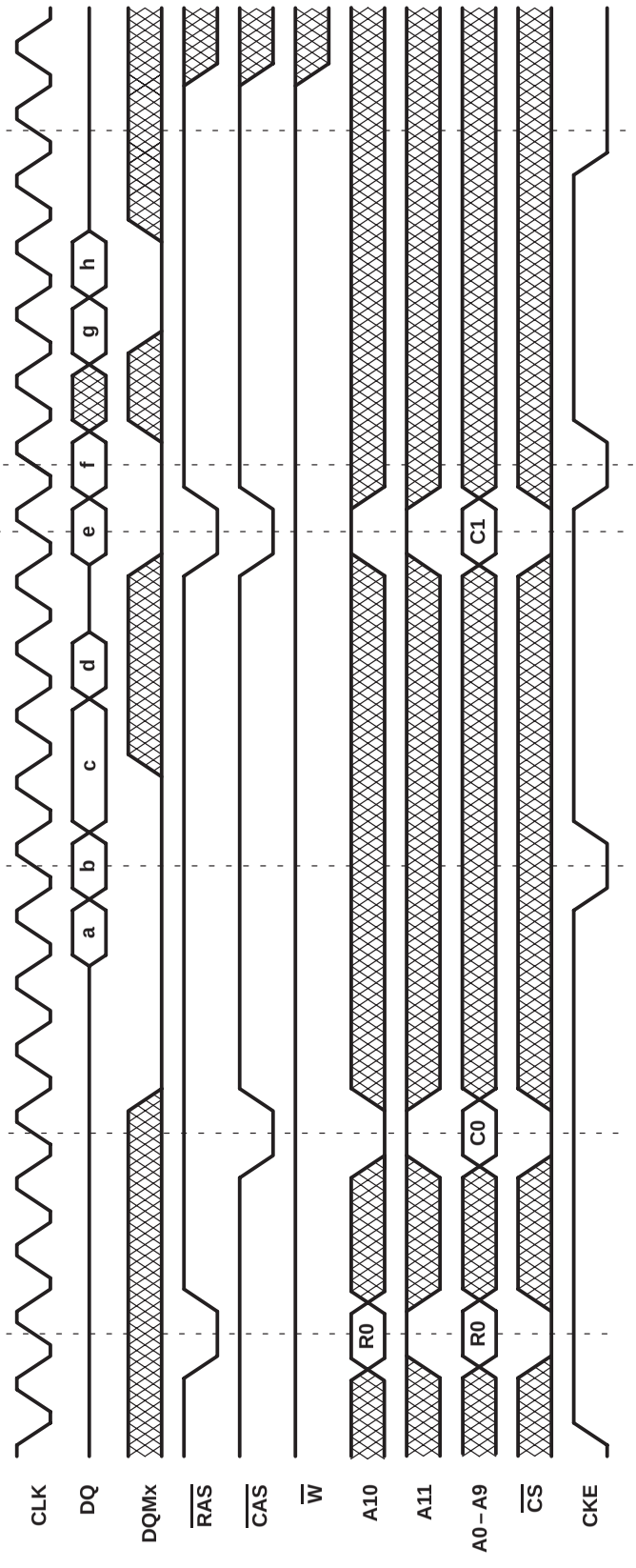
BURST TYPE	BANK	ROW	BURST CYCLE†			
(D/Q)	(B/T)	ADDR	a	b	c	d
D	B	R0	C0	C0+1	C0+2	C0+3

† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5).

NOTES: A. This example illustrates minimum t_{RP}, n_{RSA}, and t_{RCD} for the '626162-15 at 66 MHz.
B. See Figure 1.

**Figure 34. Set Mode Register (deactivate all, set mode register, write burst with automatic deactivate)
(read latency = 3, burst length = 4)**

PARAMETER MEASUREMENT INFORMATION



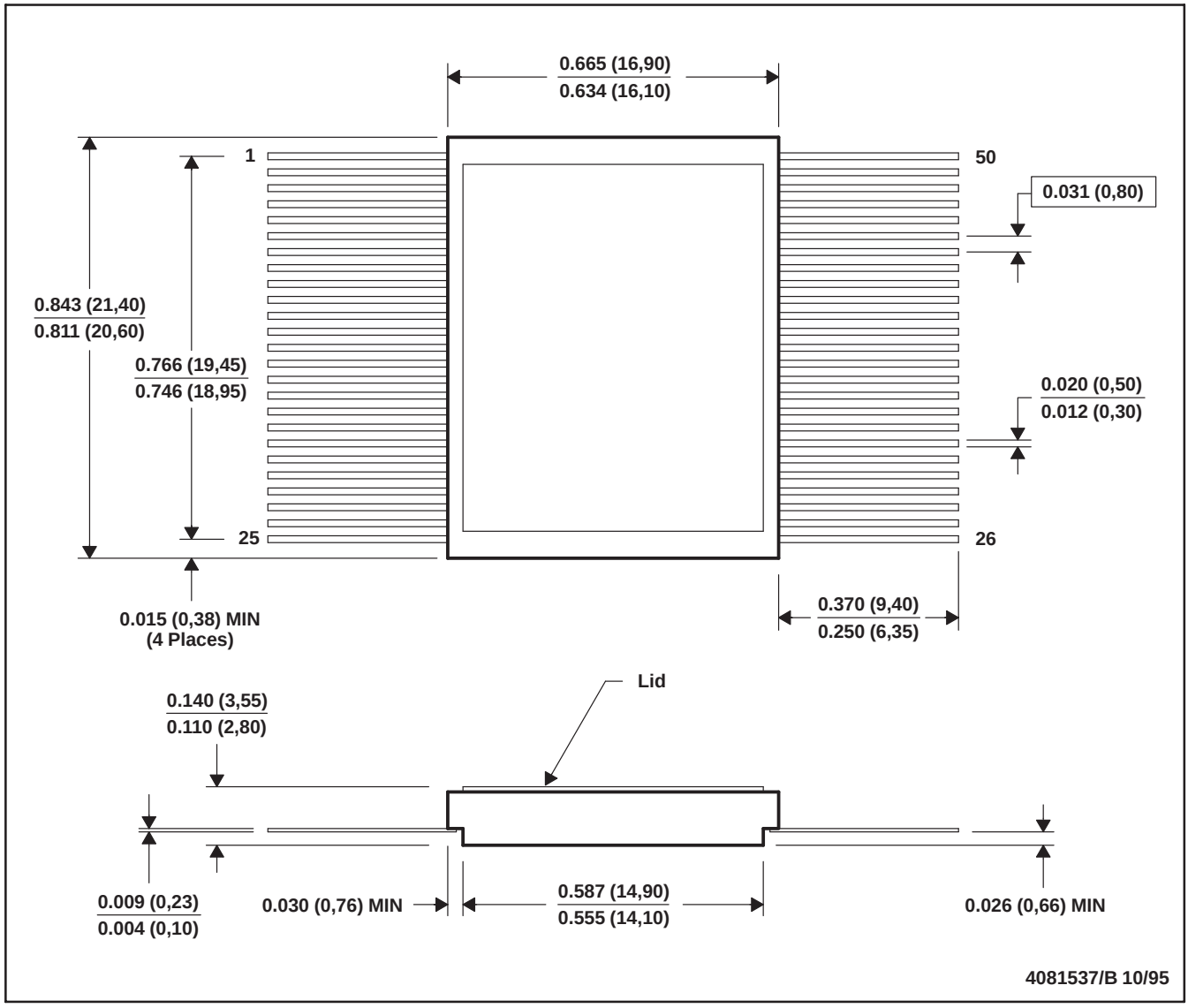
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1	C0+2	C0+3	C1	C1+1	C1+2	C1+3
D	T	R1								

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).

Figure 35. CLK Suspend (HOLD) During Read Burst and Write Burst (read latency = 3, burst length = 4)

MECHANICAL DATA

HKD (R-CDFP-F50) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The leads will be gold plated.

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