# DRAM

# 4 MEG x 1 DRAM

FAST PAGE MODE

## AVAILABLE AS MILITARY SPECIFICATONS

- SMD 5962-90622
- MIL-STD-883

## FEATURES

- Industry standard x1 pinout, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low-power, 2.5mW standby; 300mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 1,024-cycle refresh distributed across 16ms
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), and HIDDEN
- FAST PAGE MODE access cycle
- CBR with $\overline{WE}$ a HIGH (JEDEC test mode capable via WCBR)

## OPTIONS — MARKING

- Timing

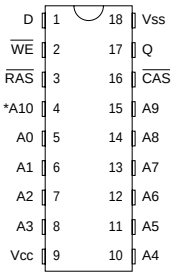
| | |
|---|---|
| 70ns access | - 7 |
| 80ns access | - 8 |
| 100ns access | -10 |
| 120ns access | -12 |

- Packages

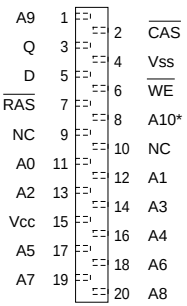
| | | |
|---|---|---|
| Ceramic DIP (300 mil) | CN | No. 101 |
| Ceramic DIP (400 mil) | C | No. 102 |
| Ceramic LCC | ECN | No. 202 |
| Ceramic SOJ | ECJ | No. 504 |
| Ceramic ZIP | CZ | No. 400 |
| Ceramic Gull Wing | ECG | No. 600 |

## PIN ASSIGNMENT (Top View)

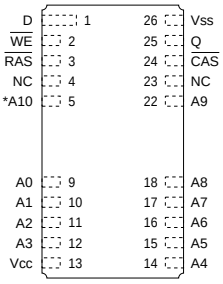
### 18-Pin DIP




### 20-Pin ZIP




### 20-Pin SOJ
### 20-Pin LCC
### 20-Pin Gull Wing



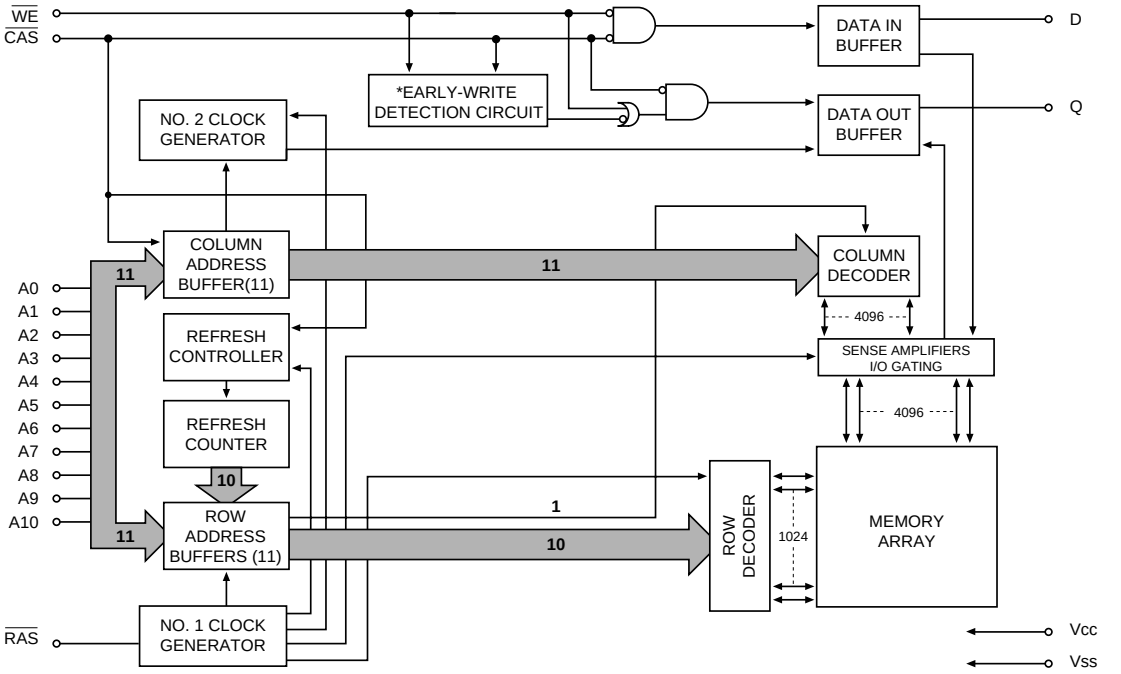

*Address not used for $\overline{RAS}$-ONLY REFRESH

## GENERAL DESCRIPTION

The MT4C1004J is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits which are entered 11 bits (A0-A10) at a time. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This LATE-$\overline{WE}$ pulse results in a READ-WRITE cycle. FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address (A0-A10) defined page

boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation. Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN REFRESH) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed at least every 16ms, regardless of sequence. The $\overline{CAS}$- BEFORE-$\overline{RAS}$ cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

## FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE




*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
$\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

## TRUTH TABLE

| FUNCTION | | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ADDRESSES | | DATA | |
|---|---|---|---|---|---|---|---|---|
| | | | | | $^tR$ | $^tC$ | D (Data In) | Q (Data Out) |
| Standby | | H | H→X | X | X | X | Don't Care | High-Z |
| READ | | L | L | H | ROW | COL | Don't Care | Data Out |
| EARLY-WRITE | | L | L | L | ROW | COL | Data In | High-Z |
| READ-WRITE | | L | L | H→L | ROW | COL | Data In | Data Out |
| FAST-PAGE-MODE | 1st Cycle | L | H→L | H | ROW | COL | Don't Care | Data Out |
| READ | 2nd Cycle | L | H→L | H | n/a | COL | Don't Care | Data Out |
| FAST-PAGE-MODE | 1st Cycle | L | H→L | L | ROW | COL | Data In | High-Z |
| EARLY-WRITE | 2nd Cycle | L | H→L | L | n/a | COL | Data In | High-Z |
| FAST-PAGE-MODE | 1st Cycle | L | H→L | H→L | ROW | COL | Data In | Data Out |
| READ-WRITE | 2nd Cycle | L | H→L | H→L | n/a | COL | Data In | Data Out |
| $\overline{RAS}$-ONLY REFRESH | | L | H | X | ROW | n/a | Don't Care | High-Z |
| HIDDEN | READ | L→H→L | L | H | ROW | COL | Don't Care | Data Out |
| REFRESH | WRITE | L→H→L | L | L | ROW | COL | Data In | High-Z |
| $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH | | H→L | L | H | X | X | Don't Care | High-Z |

## ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin Relative to $V_{SS}$ ..... -1.0V to +7.0V
Power Dissipation ..... 1W
Short Circuit Output Current ..... 50mA
Lead Temperature (Soldering 5 Seconds)..... 270°C
Storage Temperature ..... -65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (-55°C ≤ $T_A$ ≤ 125°C; $V_{CC}$ = 5V ± 10%)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V | |
| Input High (Logic 1) Voltage, All Inputs | $V_{IH}$ | 2.4 | $V_{CC}$+.5 | V | |
| Input Low (Logic 0) Voltage, All Inputs | $V_{IL}$ | -.5 | 0.8 | V | |
| INPUT LEAKAGE CURRENT<br>Any Input 0V ≤ $V_{IN}$ ≤ 5.5V VCC=5.5V<br>(All other pins not under test = 0V) | $I_I$ | -5 | 5 | µA | |
| OUTPUT LEAKAGE CURRENT (Q is Disabled, 0V ≤ $V_{OUT}$ ≤ 5.5V) VCC=5.5V | $I_{OZ}$ | -5 | 5 | µA | |
| OUTPUT LEVELS<br>Output High Voltage ($I_{OUT}$ = -5mA) | $V_{OH}$ | 2.4 | | V | |
| Output Low Voltage ($I_{OUT}$ = 4.2mA) | $V_{OL}$ | | 0.4 | V | |

| | | MAX | | | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER/CONDITION | SYMBOL | -7 | -8 | -10 | -12 | UNITS | NOTES |
| STANDBY CURRENT (TTL)<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$) | $I_{CC1}$ | 4 | 4 | 4 | 4 | mA | |
| STANDBY CURRENT (CMOS)<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{CC}$ -0.2V; all other inputs = $V_{CC}$ -0.2V) | $I_{CC2}$ | 2 | 2 | 2 | 2 | mA | |
| OPERATING CURRENT: Random READ/WRITE<br>Average Power-Supply Current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC$ = $^tRC$ (MIN)) | $I_{CC3}$ | 85 | 75 | 65 | 65 | mA | 3, 4 |
| OPERATING CURRENT: FAST PAGE MODE<br>Average Power-Supply Current<br>($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$, Address Cycling: $^tPC$ = $^tPC$ (MIN)) | $I_{CC4}$ | 60 | 50 | 45 | 40 | mA | 3, 4 |
| REFRESH CURRENT: $\overline{RAS}$-ONLY<br>Average Power-Supply Current<br>($\overline{RAS}$ Cycling, $\overline{CAS}$ = $V_{IH}$: $^tRC$ = $^tRC$ (MIN)) | $I_{CC5}$ | 85 | 75 | 65 | 65 | mA | 3 |
| REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$<br>Average Power-Supply Current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $^tRC$ = $^tRC$ (MIN)) | $I_{CC6}$ | 85 | 75 | 65 | 65 | mA | 3, 5 |

## CAPACITANCE

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance: A0-A10, D | $C_{I1}$ | | 7 | pF | 2 |
| Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | $C_{I2}$ | | 7 | pF | 2 |
| Output Capacitance: Q | $C_O$ | | 8 | pF | 2 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($-55°C \le T_C \le 125$; $V_{CC} = 5V \pm 10\%$)

| AC CHARACTERISTICS | | -7 | | -8 | | -10 | | -12 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Random READ or WRITE cycle time | $^tRC$ | 130 | | 150 | | 180 | | 220 | | ns | |
| READ-WRITE cycle time | $^tRWC$ | 155 | | 175 | | 210 | | 255 | | ns | |
| FAST-PAGE-MODE READ or WRITE cycle time | $^tPC$ | 40 | | 45 | | 55 | | 70 | | ns | |
| FAST-PAGE-MODE READ-WRITE cycle time | $^tPRWC$ | 65 | | 70 | | 85 | | 140 | | ns | |
| Access time from $\overline{RAS}$ | $^tRAC$ | | 70 | | 80 | | 90 | | 120 | ns | 14 |
| Access time from $\overline{CAS}$ | $^tCAC$ | | 20 | | 20 | | 25 | | 30 | ns | 15 |
| Access time from column address | $^tAA$ | | 35 | | 40 | | 45 | | 60 | ns | |
| Access time from $\overline{CAS}$ precharge | $^tCPA$ | | 35 | | 40 | | 45 | | 60 | ns | |
| $\overline{RAS}$ pulse width | $^tRAS$ | 70 | 10,000 | 80 | 10,000 | 100 | 10,000 | 120 | 100,000 | ns | |
| $\overline{RAS}$ pulse width (FAST PAGE MODE) | $^tRASP$ | 70 | 100,000 | 80 | 100,000 | 100 | 100,000 | 120 | 100,000 | ns | |
| $\overline{RAS}$ hold time | $^tRSH$ | 20 | | 20 | | 25 | | 30 | | ns | |
| $\overline{RAS}$ precharge time | $^tRP$ | 50 | | 60 | | 70 | | 90 | | ns | |
| $\overline{CAS}$ pulse width | $^tCAS$ | 20 | 10,000 | 20 | 10,000 | 25 | 10,000 | 30 | 10,000 | ns | |
| $\overline{CAS}$ hold time | $^tCSH$ | 70 | | 80 | | 100 | | 120 | | ns | |
| $\overline{CAS}$ precharge time | $^tCPN$ | 10 | | 10 | | 12 | | 15 | | ns | 16 |
| $\overline{CAS}$ precharge time (FAST PAGE MODE) | $^tCP$ | 10 | | 10 | | 12 | | 15 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $^tRCD$ | 20 | 50 | 20 | 60 | 25 | 75 | 25 | 90 | ns | 17 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $^tCRP$ | 5 | | 5 | | 5 | | 10 | | ns | |
| Row address setup time | $^tASR$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Row address hold time | $^tRAH$ | 10 | | 10 | | 15 | | 15 | | ns | |
| $\overline{RAS}$ to column address delay time | $^tRAD$ | 15 | 35 | 15 | 40 | 20 | 50 | 20 | 60 | ns | 18 |
| Column address setup time | $^tASC$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Column address hold time | $^tCAH$ | 15 | | 20 | | 25 | | 25 | | ns | |
| Column address hold time (referenced to $\overline{RAS}$) | $^tAR$ | 50 | | 60 | | 70 | | 85 | | ns | |
| Column address to $\overline{RAS}$ lead time | $^tRAL$ | 35 | | 40 | | 50 | | 60 | | ns | |
| Read command setup time | $^tRCS$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Read command hold time (referenced to $\overline{CAS}$) | $^tRCH$ | 0 | | 0 | | 0 | | 0 | | ns | 19 |
| Read command hold time (referenced to $\overline{RAS}$) | $^tRRH$ | 0 | | 0 | | 0 | | 0 | | ns | 19 |
| $\overline{CAS}$ to output in Low-Z | $^tCLZ$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Output buffer turn-off delay | $^tOFF$ | 0 | 20 | 0 | 20 | 0 | 20 | 0 | 20 | ns | 20 |
| $\overline{WE}$ command setup time | $^tWCS$ | 0 | | 0 | | 0 | | 0 | | ns | 21 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

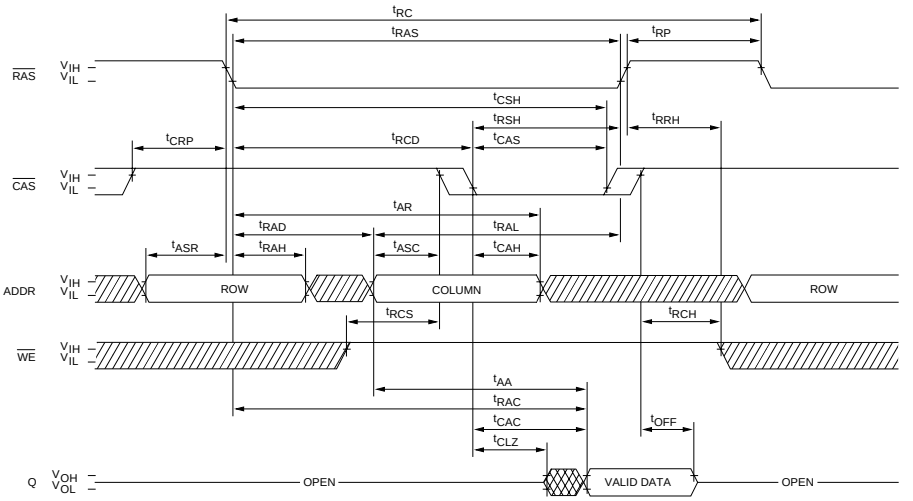
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ $T_C$ ≤ 125; Vcc = 5V ± 10%)

| AC CHARACTERISTICS | | -7 | | -8 | | -10 | | -12 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Write command hold time | $^tWCH$ | 15 | | 15 | | 20 | | 25 | | ns | |
| Write command hold time (referenced to $\overline{RAS}$) | $^tWCR$ | 50 | | 60 | | 70 | | 85 | | ns | |
| Write command pulse width | $^tWP$ | 15 | | 15 | | 20 | | 25 | | ns | |
| Write command to $\overline{RAS}$ lead time | $^tRWL$ | 20 | | 20 | | 25 | | 30 | | ns | |
| Write command to $\overline{CAS}$ lead time | $^tCWL$ | 20 | | 20 | | 25 | | 30 | | ns | |
| Data-in setup time | $^tDS$ | 0 | | 0 | | 0 | | 0 | | ns | 22 |
| Data-in hold time | $^tDH$ | 12 | | 15 | | 18 | | 25 | | ns | 22 |
| Data-in hold time (referenced to $\overline{RAS}$) | $^tDHR$ | 50 | | 60 | | 70 | | 90 | | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $^tRWD$ | 70 | | 80 | | 100 | | 120 | | ns | 21 |
| Column address to $\overline{WE}$ delay time | $^tAWD$ | 35 | | 40 | | 50 | | 60 | | ns | 21 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $^tCWD$ | 20 | | 20 | | 25 | | 30 | | ns | 21 |
| Transition time (rise or fall) | $^tT$ | 3 | 50 | 3 | 50 | 3 | 50 | 3 | 50 | ns | |
| Refresh period (1,024 cycles) | $^tREF$ | | 16 | | 16 | | 16 | | 16 | ms | |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | $^tRPC$ | 0 | | 0 | | 0 | | 0 | | ns | |
| $\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH) | $^tCSR$ | 10 | | 10 | | 10 | | 10 | | ns | 5 |
| $\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH) | $^tCHR$ | 10 | | 15 | | 20 | | 25 | | ns | 5 |
| $\overline{WE}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH) | $^tWRH$ | 10 | | 10 | | 10 | | 10 | | ns | 24, 25 |
| $\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH) | $^tWRP$ | 10 | | 10 | | 10 | | 10 | | ns | 24, 25 |
| $\overline{WE}$ hold time (WCBR test cycle) | $^tWTH$ | 10 | | 10 | | 10 | | 10 | | ns | 24, 25 |
| $\overline{WE}$ setup time (WCBR test cycle) | $^tWTS$ | 10 | | 10 | | 10 | | 10 | | ns | 24, 25 |

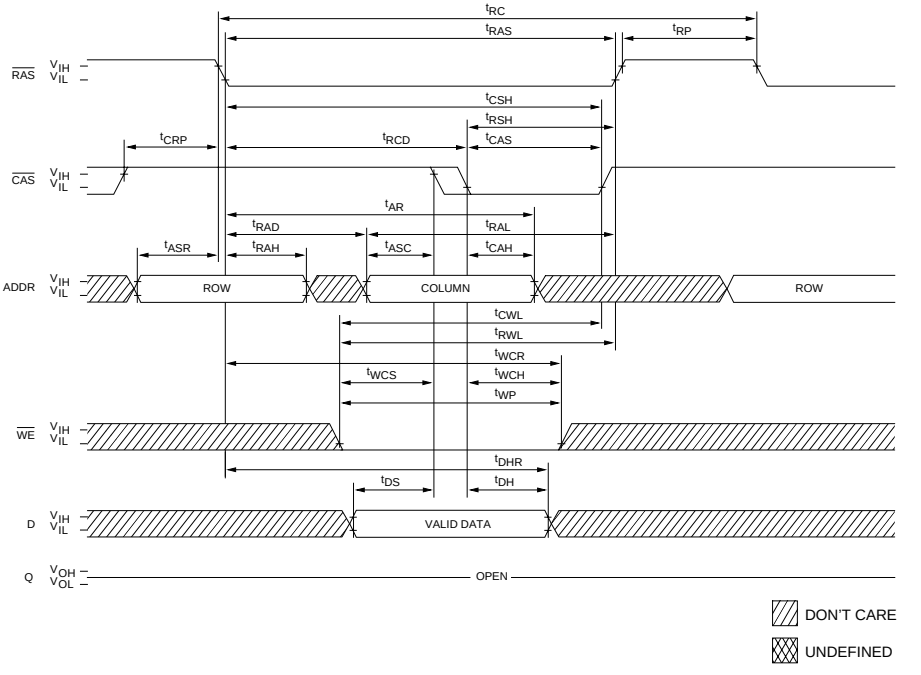
## NOTES

1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled, not 100% tested. Capacitance is measured with Vcc = 5V, f = 1 MHz at less than 50mVrms, $T_A$ = 25°C ±3°C, Vbias = 2.4V applied to each input and output individually with remaining inputs and outputs open.
3. $I_{CC}$ is dependent on cycle rates.
4. $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ $T_A$ ≤ 125°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
8. AC characteristics assume $^tT$ = 5ns.
9. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
10. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
11. If $\overline{CAS}$ = $V_{IH}$, data output is High-Z.
12. If $\overline{CAS}$ = $V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If $^tRCD$ is greater than the maximum recommended value shown in this table, $^tRAC$ will increase by the amount that $^tRCD$ exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for $^tCPN$.
17. Operation within the $^tRCD$ (MAX) limit ensures that $^tRAC$ (MAX) can be met. $^tRCD$ (MAX) is specified as a reference point only; if $^tRCD$ is greater than the specified $^tRCD$ (MAX) limit, then access time is controlled exclusively by $^tCAC$.
18. Operation within the $^tRAD$ (MAX) limit ensures that $^tRCD$ (MAX) can be met. $^tRAD$ (MAX) is specified as a reference point only; if $^tRAD$ is greater than the specified $^tRAD$ (MAX) limit, then access time is controlled exclusively by $^tAA$.
19. Either $^tRCH$ or $^tRRH$ must be satisfied for a READ cycle.
20. $^tOFF$ (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to $V_{OH}$ or $V_{OL}$.
21. $^tWCS$, $^tRWD$, $^tAWD$ and $^tCWD$ are restrictive operating parameters in LATE WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the cycle is a LATE-WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to $V_{IH}$).
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW.
24. $^tWTS$ and $^tWTH$ are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of $^tWRP$ and $^tWRH$ in the CBR REFRESH cycle.
25. JEDEC test mode only.

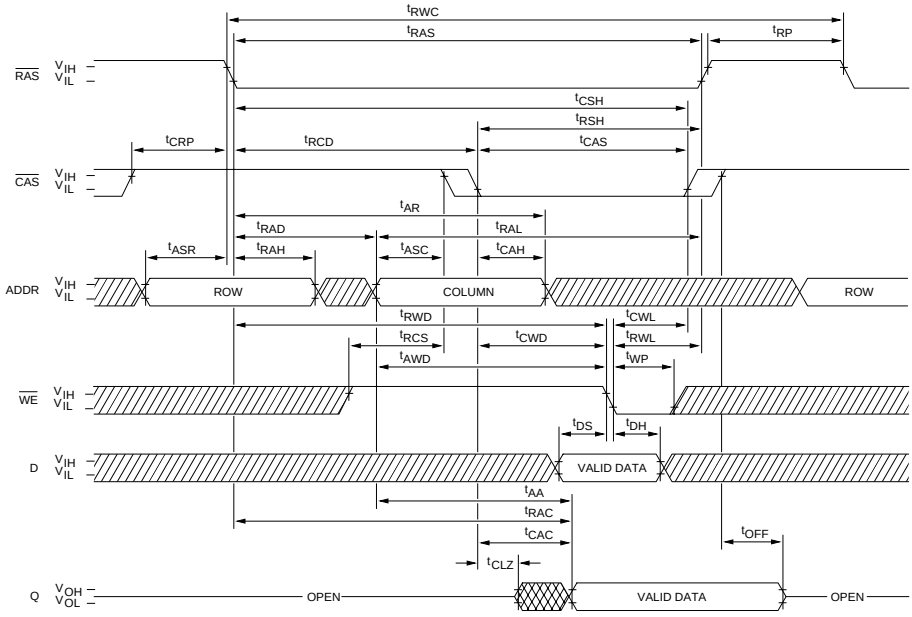
## READ CYCLE



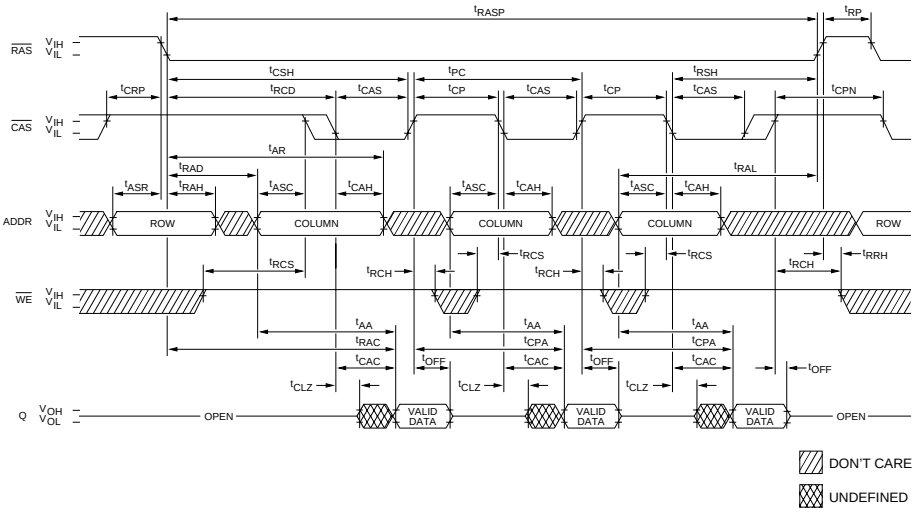

## EARLY-WRITE CYCLE



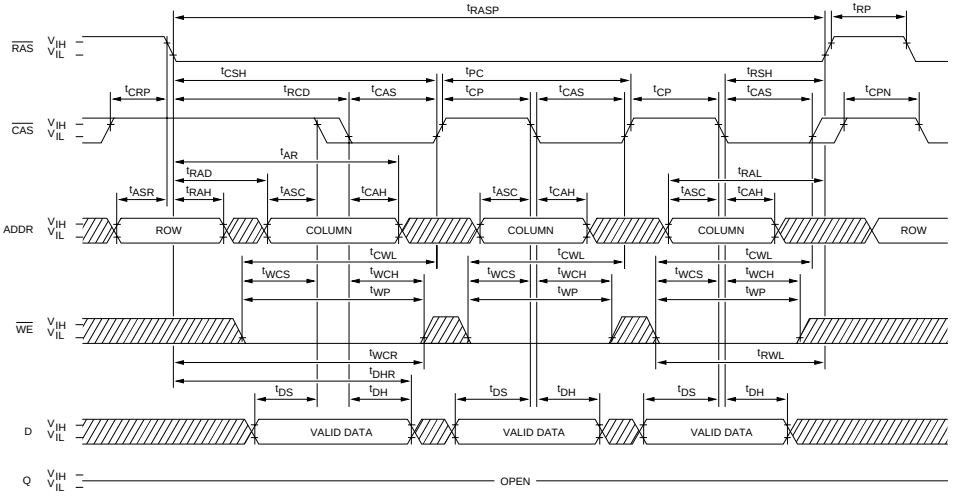
## READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



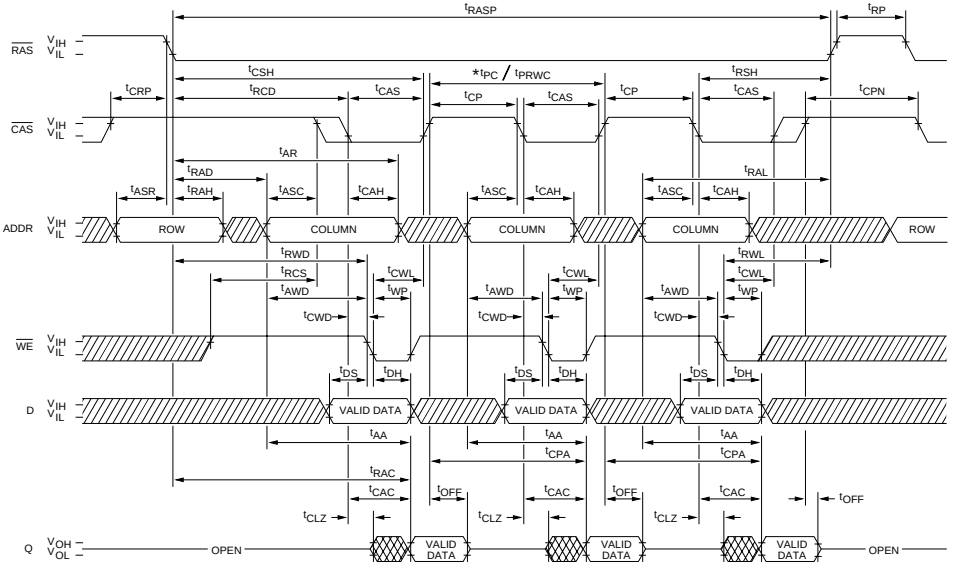

## FAST-PAGE-MODE READ CYCLE



## FAST-PAGE-MODE EARLY-WRITE CYCLE



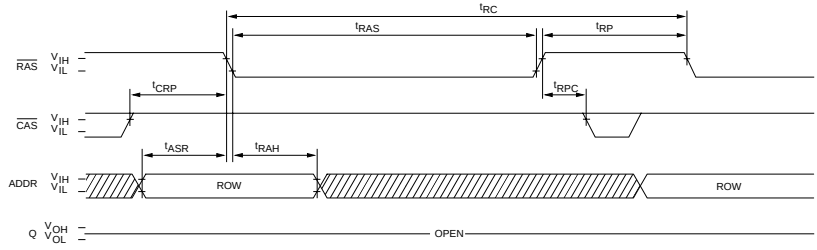

## FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)




*tPC = LATE-WRITE Cycle
tPRWC = FAST READ-MODIFY-WRITE Cycle

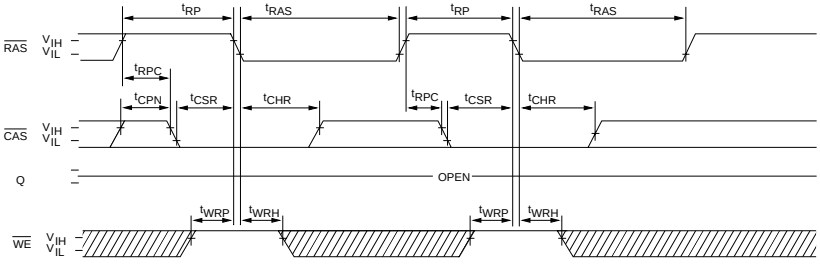
## $\overline{\text{RAS}}$-ONLY REFRESH CYCLE

(ADDR = A0-A9; A10 and $\overline{\text{WE}}$ = DON'T CARE)



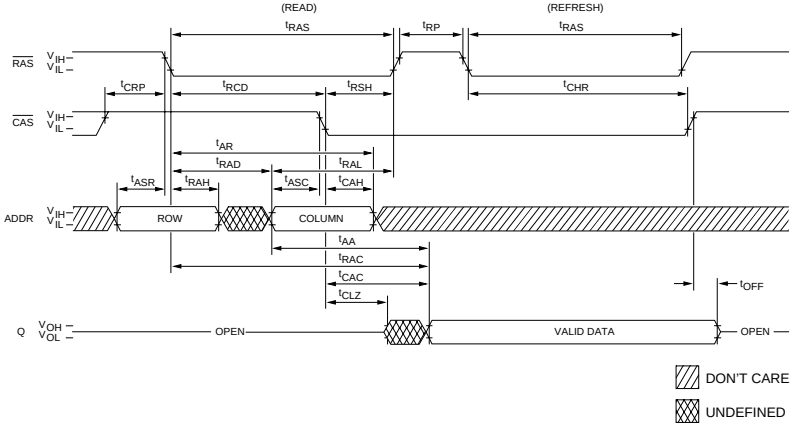

## $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

(A0-A10 = DON'T CARE)




## HIDDEN REFRESH CYCLE [23]

($\overline{\text{WE}}$ = HIGH)



## 4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA / JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

## REFRESH

The most commonly used refresh mode of the 1 Meg is the CBR ($\overline{CAS}$-BEFORE-$\overline{RAS}$) REFRESH cycle. The CBR for the 1 Meg specifies the $\overline{WE}$ pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the $\overline{WE}$ pin held at a voltage HIGH level.

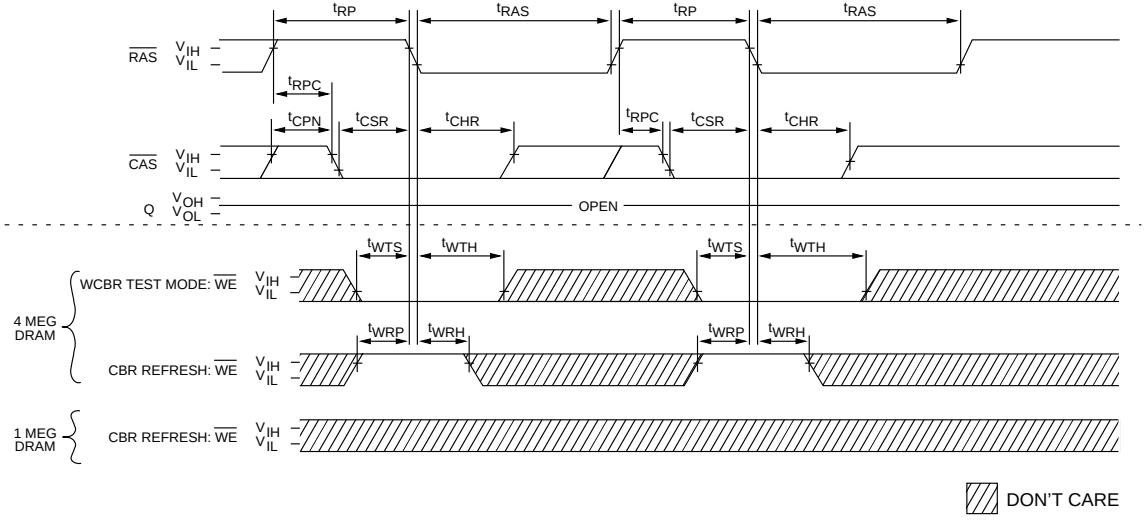
A CBR cycle with $\overline{WE}$ LOW will put the 4 Meg into the JEDEC specified test mode (WCBR).

## POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100µs delay followed by any eight $\overline{RAS}$ cycles. The 4 Meg POWER-UP is more restrictive in that eight $\overline{RAS}$-ONLY or CBR REFRESH ($\overline{WE}$ held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a $\overline{RAS}$-ONLY or a CBR REFRESH cycle ($\overline{WE}$ held HIGH).

## SUMMARY

1. The 1 Meg CBR REFRESH allows the $\overline{WE}$ pin to be "don't care" while the 4 Meg CBR requires $\overline{WE}$ to be HIGH.
2. The eight $\overline{RAS}$ wake-up cycles on the 1 Meg may be any valid $\overline{RAS}$ cycle while the 4 Meg may only use $\overline{RAS}$-ONLY or CBR REFRESH cycles ($\overline{WE}$ held HIGH).




### COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR

## ELECTRICAL TEST REQUIREMENTS

| MIL-STD-883 TEST REQUIREMENTS | SUBGROUPS (per Method 5005, Table I) |
|---|---|
| INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004) | 2, 8A, 10 |
| FINAL ELECTRICAL TEST PARAMETERS (Method 5004) | 1*, 2, 3, 7*, 8, 9, 10, 11 |
| GROUP A TEST REQUIREMENTS (Method 5005) | 1, 2, 3, 4**, 7, 8, 9, 10, 11 |
| GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005) | 1, 2, 3, 7, 8, 9, 10, 11 |

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.