

**128K x 8 SRAM**  
RUGGEDIZED PLASTIC  
HIGH SPEED SRAM

**FEATURES**

- Access times of 15, 20, 25 and 35 ns
- Fast output enable ( $t_{AOE}$ ) for cache applications
- Low active power
- Low standby power
- Fully static operation, no clock or refresh required
- TTL Compatible Inputs and Outputs
- Single +5V power supply
- Package in Industry-standard 32-pin SOJ

**OPTIONS**

- Timing

|             |     |
|-------------|-----|
| 15ns access | -15 |
| 20ns access | -20 |
| 25ns access | -25 |
| 35ns access | -35 |

- Package

|              |            |
|--------------|------------|
| Plastic SOJ* | DJ_No. 905 |
|--------------|------------|

- Operating Temperature Ranges

|                              |    |
|------------------------------|----|
| -Military (-55°C to +125°C)  | XT |
| -Industrial (-40°C to +85°C) | IT |

**GENERAL DESCRIPTION**

The AS5C1008 is a high speed, low power, 128K by 8-bit ruggedized plastic (COTS) CMOS Static RAM. It is fabricated using high performance, CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 15ns (Max) over the military and industrial temperature ranges.

When Chip Enable (CE\ ) is HIGH, the device assumes a standby mode at which the power dissipation can be reduced down to 125mW (max) at CMOS input levels.

Easy memory expansion is provided by using asserted LOW CE\ and asserted HIGH CE2, and asserted LOW write enable (WE\ ) controls both writing and reading of the memory.

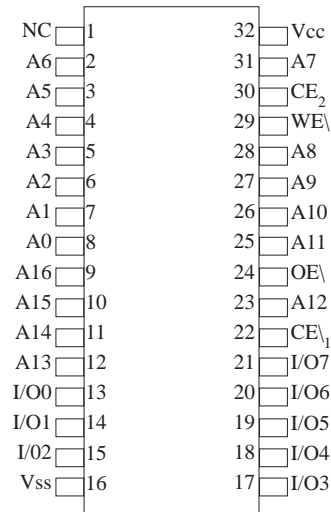
The AS5C1008 is pin-compatible with other 128K x 8 SRAM's in the SOJ package.

*\*For ceramic versions of this product, please see the MT5C1008 datasheet.*

**PIN ASSIGNMENT**

(Top View)

32-Pin Plastic SOJ (DJ)



**PIN FUNCTIONS**

|             |                     |
|-------------|---------------------|
| A0 - A16    | Address Inputs      |
| WE\         | Write Enable        |
| CE\1, CE2   | Chip Enable         |
| OE\         | Output Enable       |
| I/O0 - I/O7 | Data Inputs/Outputs |
| VCC         | Power               |
| VSS         | Ground              |
| NC          | No Connection       |

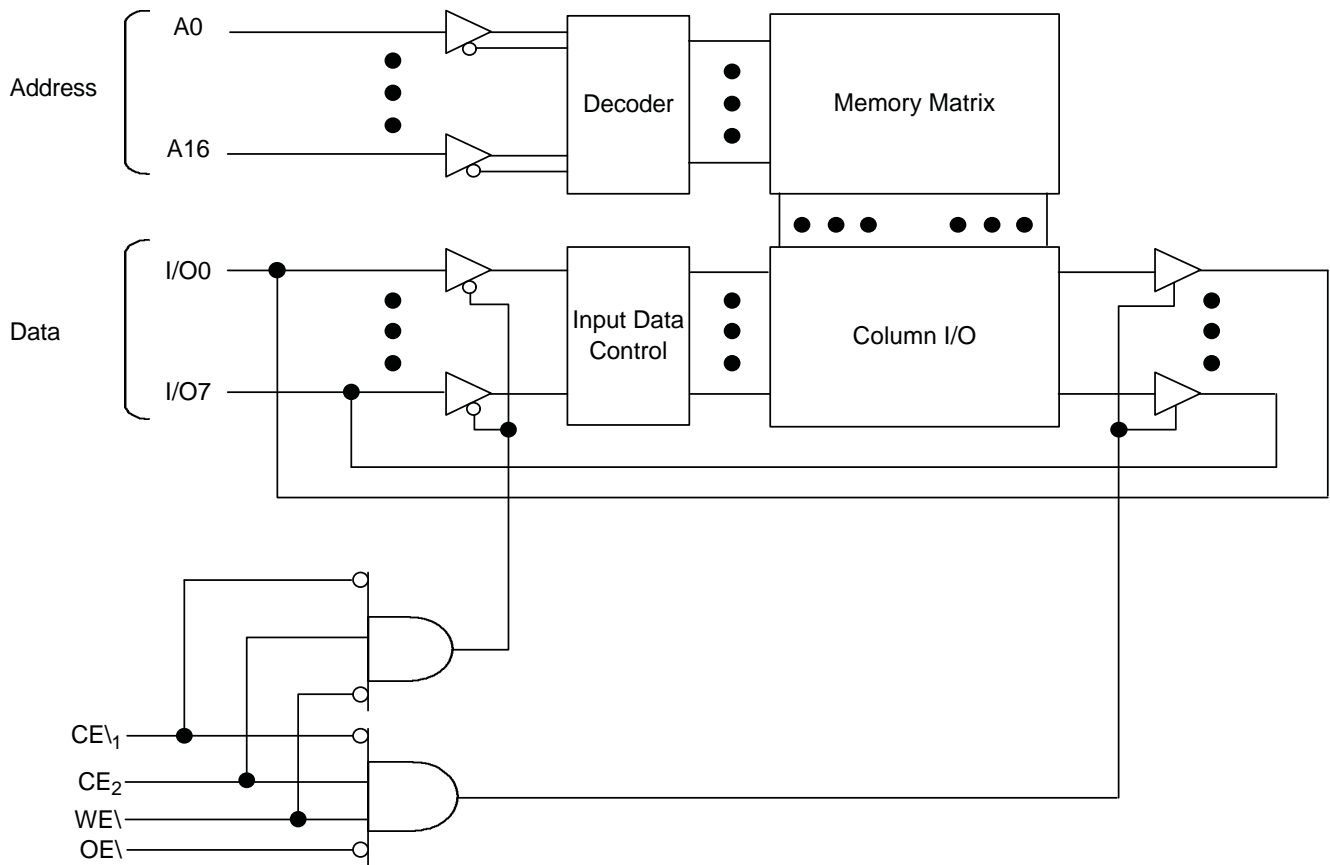
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**ABSOLUTE MAXIMUM RATINGS\***

|   |                    |
|---|--------------------|
| Vcc Supply Relative to GND.....             | -0.5V to +7.0V     |
| Voltage on any pin Relative to GND.....     | -0.5V to Vcc +7.0V |
| Storage Temperature .....                   | -65°C to +150°C    |
| Ambient Temperature with Power Applied..... | -55°C to +125°C    |
| Short Circuit Output Current.....           | 260°C              |
| Power Dissipation.....                      | 1.0W               |

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**FUNCTIONAL BLOCK DIAGRAM**



## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

( $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{CC} = 5V \pm 10\%$ )

| PARAMETER                             | CONDITIONS   | SYMBOL    | -15  |                | -20  |                | -25  |                | -35  |                | UNITS         |
|---------------------------------------|--|-----------|------|----------------|------|----------------|------|----------------|------|----------------|---------------|
|                                       |  |           | MIN  | MAX            | MIN  | MAX            | MIN  | MAX            | MIN  | MAX            |               |
| Dynamic Operating Current             | $V_{CC} = \text{MAX}$ , $I_{OUT} = 0\text{mA}$ ,<br>$CE_1 = V_{IL}$ and $CE_2 = V_{IH}$ , $f = f_{max}$  | $I_{CC1}$ |      | 180            |      | 150            |      | 140            |      | 125            | mA            |
| TTL Standby Current -<br>TTL Inputs   | $V_{CC} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ ,<br>$CE_1 \geq V_{IH}$ and $CE_2 \geq V_{IL}$ , $f = f_{max}$                           | $I_{SB1}$ |      | 90             |      | 75             |      | 70             |      | 60             | mA            |
| CMOS Standby Current -<br>CMOS Inputs | $V_{CC} = \text{MAX}$ , $CE_1 \geq V_{CC} - 0.2V$ , or $CE_2$<br>$\leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ and<br>$V_{IN} \leq 0.2V$ , $f = 0$ | $I_{SB2}$ |      | 10             |      | 10             |      | 10             |      | 10             | mA            |
| Input Leakage Current                 | $GND \leq V_{IN} \leq V_{CC}$  | $I_{LI}$  | -10  | 10             | -10  | 10             | -10  | 10             | -10  | 10             | $\mu\text{A}$ |
| Output Leakage Current                | $GND \leq V_{OUT} \leq V_{CC}$<br>Output Disabled  | $I_{LO}$  | -10  | 10             | -10  | 10             | -10  | 10             | -10  | 10             | $\mu\text{A}$ |
| Output High Voltage                   | $V_{CC} = \text{MIN}$ , $I_{OH} = -4.0\text{mA}$   | $V_{OH}$  | 2.4  |                | 2.4  |                | 2.4  |                | 2.4  |                | V             |
| Output Low Voltage                    | $V_{CC} = \text{MIN}$ , $I_{OL} = 8.0\text{mA}$  | $V_{OL}$  |      | 0.4            |      | 0.4            |      | 0.4            |      | 0.4            | V             |
| Input High Voltage                    |  | $V_{IH}$  | 2.2  | $V_{CC} + 0.5$ | 2.2  | $V_{CC} + 0.5$ | 2.2  | $V_{CC} + 0.5$ | 2.2  | $V_{CC} + 0.5$ | V             |
| Input Low Voltage                     |  | $V_{IL}$  | -0.5 | 0.8            | -0.5 | 0.8            | -0.5 | 0.8            | -0.5 | 0.8            | V             |

### PIN DESCRIPTIONS

#### A0 - A16: Address Inputs

These 17 address inputs select one of the 131,072 8-bit words in the RAM.

#### $CE_1$ : Chip Enable 1 Input

$CE_1$  is asserted LOW to read from or write to the device. If Chip Enable 1 is deasserted, the device is deselected and is in standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

#### $CE_2$ : Chip Enable 2 Input

$CE_2$  is asserted HIGH to read from or write to the device. If Chip Enable 2 is deasserted, the device is deselected and is in standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

#### $OE$ : Output Enable Input

The Output Enable Input is asserted LOW. If asserted LOW while  $CE_1$  is asserted (LOW) and  $CE_2$  is asserted (HIGH) and  $WE$  is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the high-impedance state when  $OE$  is deasserted.

#### $WE$ : Write Enable Input

The Write Enable input is asserted LOW and controls read and write operations. When  $CE_1$  and  $WE$  are both asserted (LOW) and  $CE_2$  is asserted (HIGH) input data present on the I/O pins will be written into the selected memory location.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

 (-55°C ≤ T<sub>A</sub> ≤ +125°C or -40°C to +85°C; V<sub>CC</sub> = 5V ± 10%)

| DESCRIPTION                                 | SYMBOL <sup>1</sup> | -15 |     | -20 |     | -25 |     | -35 |     | UNIT |
|---|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|------|
|   |                     | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |      |
| <b>READ CYCLE</b>                           |                     |     |     |     |     |     |     |     |     |      |
| Read Cycle Time                             | t <sub>RC</sub>     | 15  |     | 20  |     | 25  |     | 35  |     | ns   |
| Address Access Time                         | t <sub>AA</sub>     |     | 15  |     | 20  |     | 25  |     | 35  | ns   |
| Chip Enable Access Time                     | t <sub>ACE</sub>    |     | 15  |     | 20  |     | 25  |     | 35  | ns   |
| Output Hold from Address Change             | t <sub>OH</sub>     | 3   |     | 3   |     | 3   |     | 3   |     | ns   |
| Chip Enable to Output in Low-Z              | t <sub>LZCE</sub>   | 3   |     | 3   |     | 3   |     | 3   |     | ns   |
| Chip Disable to Output in High-Z            | t <sub>HZCE</sub>   |     | 7   |     | 8   |     | 10  |     | 15  | ns   |
| Output Enable Access Time                   | t <sub>AOE</sub>    |     | 7   |     | 7   |     | 10  |     | 15  | ns   |
| Output Enable to Output in Low-Z            | t <sub>LZOE</sub>   | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| Output Disable to Output in High-Z          | t <sub>HZOE</sub>   |     | 7   |     | 8   |     | 10  |     | 15  | ns   |
| <b>WRITE CYCLE</b>                          |                     |     |     |     |     |     |     |     |     |      |
| Write Cycle Time                            | t <sub>WC</sub>     | 15  |     | 20  |     | 25  |     | 35  |     | ns   |
| Chip Enable to End of Write                 | t <sub>CW</sub>     | 12  |     | 15  |     | 20  |     | 25  |     | ns   |
| Address Valid to End of Write               | t <sub>AW</sub>     | 12  |     | 15  |     | 20  |     | 25  |     | ns   |
| Address Set-up Time                         | t <sub>AS</sub>     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| Address Hold from End of Write              | t <sub>AH</sub>     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| Write Pulse Width (OE \ ≥ V <sub>IH</sub> ) | t <sub>WP</sub>     | 12  |     | 15  |     | 20  |     | 30  |     | ns   |
| Data Set-up Time                            | t <sub>DS</sub>     | 8   |     | 10  |     | 15  |     | 20  |     | ns   |
| Data Hold Time                              | t <sub>DH</sub>     | 0   |     | 0   |     | 0   |     | 0   |     | ns   |
| Write Disable to Output in Low-Z            | t <sub>LZWE</sub>   | 5   |     | 5   |     | 5   |     | 5   |     | ns   |
| Write Enable to Output in High-Z            | t <sub>HZWE</sub>   |     | 7   |     | 9   |     | 10  |     | 15  | ns   |

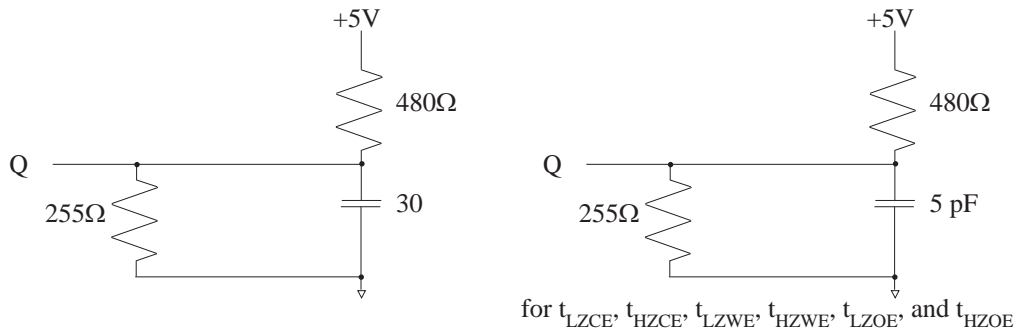
**NOTE:** 1. t<sub>LZCE</sub>, t<sub>LZWE</sub>, t<sub>HZCE</sub>, t<sub>LZOE</sub>, and t<sub>HZOE</sub> are simulated values.

**CAPACITANCE** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

| PARAMETER          | CONDITION      | SYMBOL    | MAX | UNIT |
|--------------------|----------------|-----------|-----|------|
| Input Capacitance  | $V_{IN} = 0V$  | $C_{IN}$  | 6   | pF   |
| Output Capacitance | $V_{OUT} = 0V$ | $C_{OUT}$ | 8   | pF   |

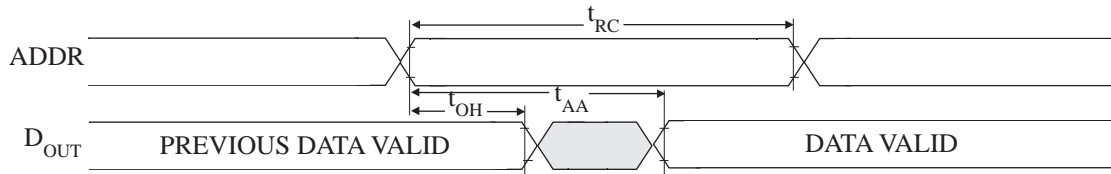
**AC TEST CONDITIONS**

|                                    |              |
|------------------------------------|--------------|
| Input Pulse Levels.....            | GND to 3.0V  |
| Input Rise and Fall Times.....     | 3ns          |
| Input Timing Reference Levels..... | 1.5V         |
| Output Reference Levels.....       | 1.5V         |
| Output Load.....                   | See Figure 1 |



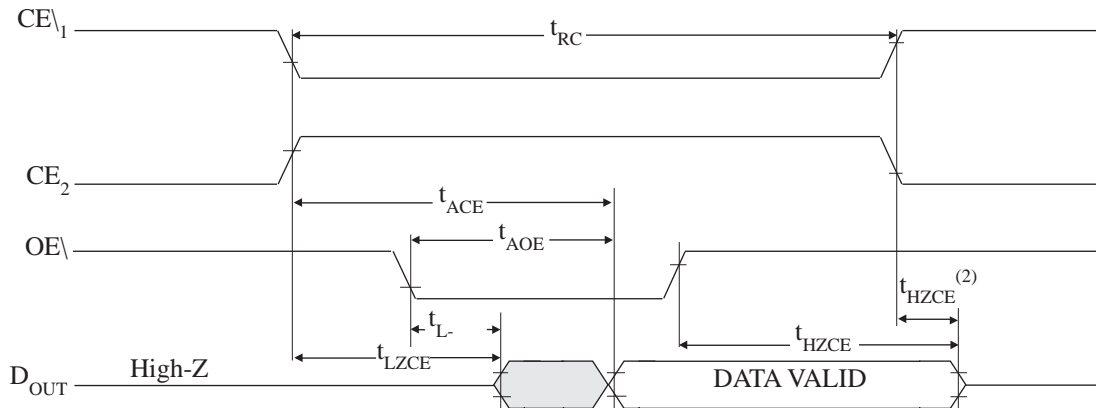
**Fig. 1 OUTPUT LOAD EQUIVALENT**

### READ CYCLE TIMING 1<sup>(1)</sup>



**NOTE:** 1. CE $\setminus$  is HIGH for READ cycle.

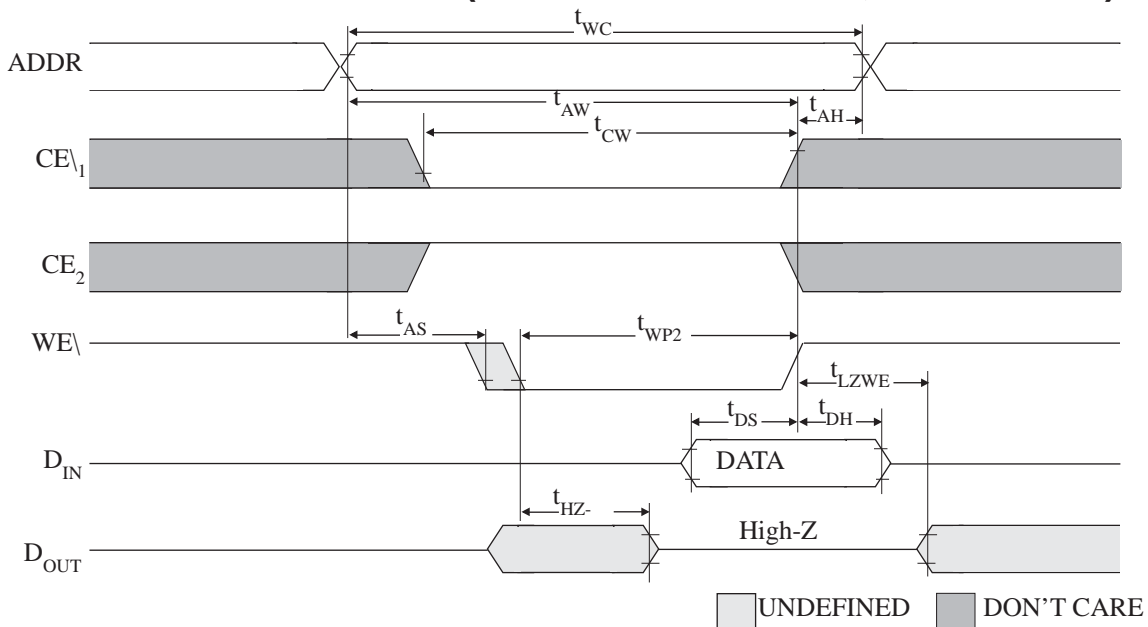
### READ CYCLE TIMING 2<sup>(1)</sup>



**NOTES:** 1. CE $\setminus$  is HIGH for READ cycle.

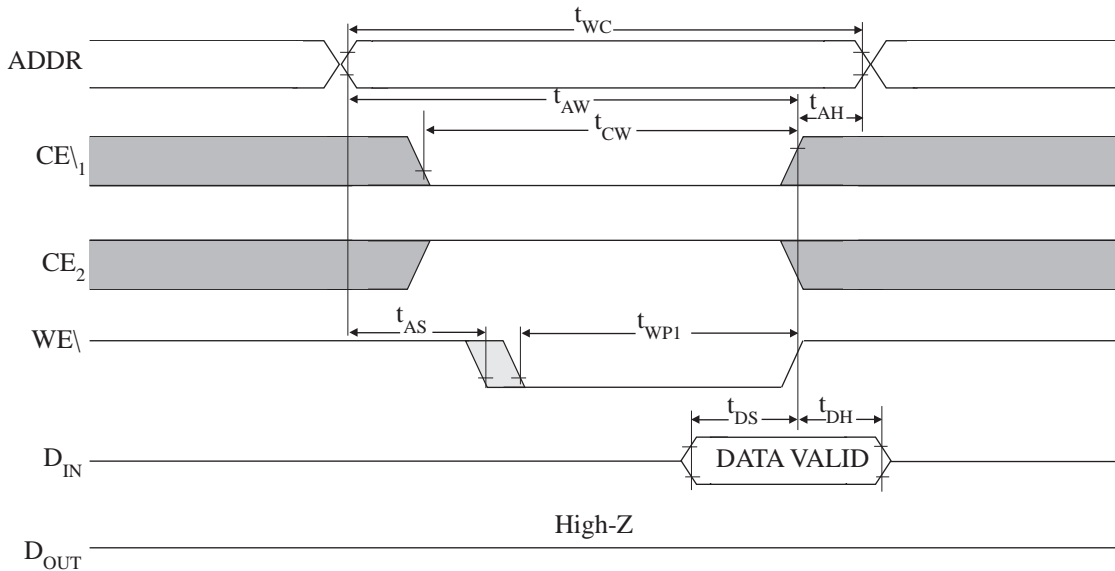
2. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ .

### WRITE CYCLE TIMING (WE $\setminus$ CONTROLLED, OE $\setminus$ = LOW)

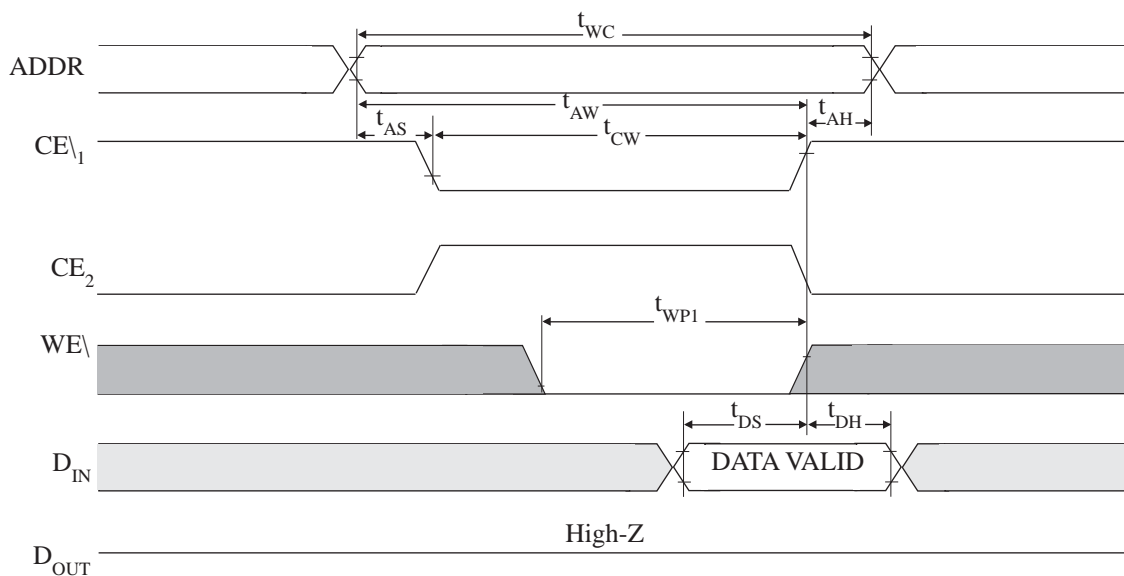


□ UNDEFINED    ■ DON'T CARE

### WRITE CYCLE TIMING (CE<sub>1</sub> CONTROLLED, OE<sub>1</sub> = LOW)



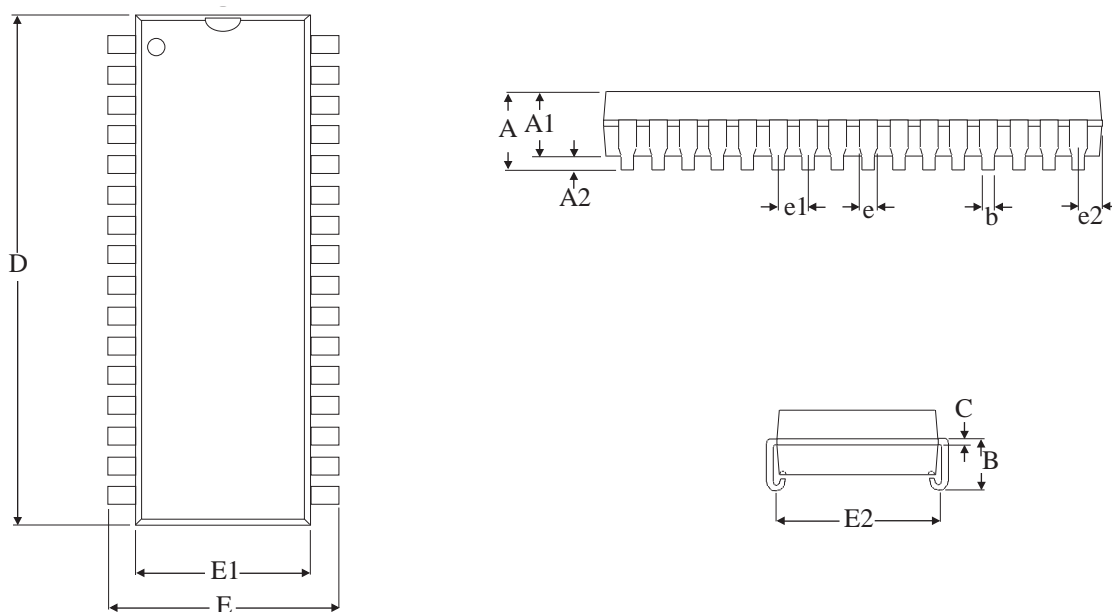
### WRITE CYCLE TIMING (CE<sub>2</sub> CONTROLLED, OE<sub>1</sub> = LOW)



□ UNDEFINED    ■ DON'T CARE

## MECHANICAL DEFINITION\*

Micross Case #905 (Package Designator DJ)



| SYMBOL | MICROSS PACKAGE SPECIFICATIONS |       |
|--------|--------------------------------|-------|
|        | MIN                            | MAX   |
| A      | 0.140 BSC                      |       |
| A1     | 0.105                          | 0.115 |
| A2     | 0.027 TYP                      |       |
| B      | 0.082                          | ---   |
| b      | 0.018 TYP                      |       |
| C      | 0.010 TYP                      |       |
| D      | 0.820                          | 0.880 |
| E      | 0.430                          | 0.445 |
| E1     | 0.395                          | 0.405 |
| E2     | 0.360                          | 0.380 |
| e      | 0.025                          | 0.032 |
| e1     | 0.050 TYP                      |       |
| e2     | ---                            | 0.045 |

\* All measurements are in inches.



## ORDERING INFORMATION

**EXAMPLE:** AS5C1008DJ-25/XT

| Device Number | Package Type | Speed ns | Process |
|---------------|--------------|----------|---------|
| AS5C1008      | DJ           | -15      | /*      |
| AS5C1008      | DJ           | -20      | /*      |
| AS5C1008      | DJ           | -25      | /*      |
| AS5C1008      | DJ           | -35      | /*      |

### \*AVAILABLE PROCESSES

IT = Industrial Temperature Range

-40°C to +85°C

XT = Extended Temperature Range

-55°C to +125°C

**DOCUMENT TITLE**

**128K x 8 SRAM RUGGEDIZED PLASTIC HIGH SPEED SRAM**

**REVISION HISTORY**

| <u>Rev #</u> | <u>History</u>              | <u>Release Date</u> | <u>Status</u> |
|--------------|-----------------------------|---------------------|---------------|
| 3.7          | Updated AC & DC Specs       | March 2009          | Release       |
| 3.8          | Updated Micross Information | January 2010        | Release       |
| 3.9          | Updated Order Chart         | October 2010        | Release       |