

## 128K x 8 EEPROM

EEPROM Memory

5 Volt, Byte Alterable

### AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-38267
- MIL-STD-883

### FEATURES

- Access speed: 120, 150, 200, and 250ns
- Data Retention: 100 Years
- Low power, active current: 50mA, standby current: 500uA
- Single +5V ( $\pm 10\%$ ) power supply
- Data Polling and Toggle Bit
- Erase/Write Endurance (10,000 byte mode / 100,000 page mode)
- Software Data protection Algorithm
- Data Protection Circuitry during power on/off
- Hardware Data Protection
- Automatic , Self-Timed Byte Write
- Automatic Programming:  
Automatic Page Write: 10ms (MAX)

### OPTIONS

- Timing
 

120ns access	-12
150ns access	-15
200ns access	-20
250ns access	-25
- Packages
 

Ceramic Flat Pack	F
CerDIP, 600 mil	CW
- Operating Temperature Ranges
 

-Military (-55°C to +125°C)	XT
-Industrial (-40°C to +85°C)	IT
-Full Military Processing	Q

**NOTE:** Package lid is connected to ground (Vss).

### GENERAL DESCRIPTION

The AS28C010 is a 1 Megabit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 131, 072 x 8 bits. The AS28C010 is capable of in system electrical Byte and Page reprogrammability.

The AS28C010 achieves high speed access, low power consumption, and a high level of reliability by employing advanced CMOS process and circuitry technology.

This device has a 256-Byte Page Programming function to make its erase and write operations faster. The AS28C010 features Data Polling and Toggle Bit to indicate completion of erase and programming operations.

This EEPROM provides several levels of data protection. Hard-

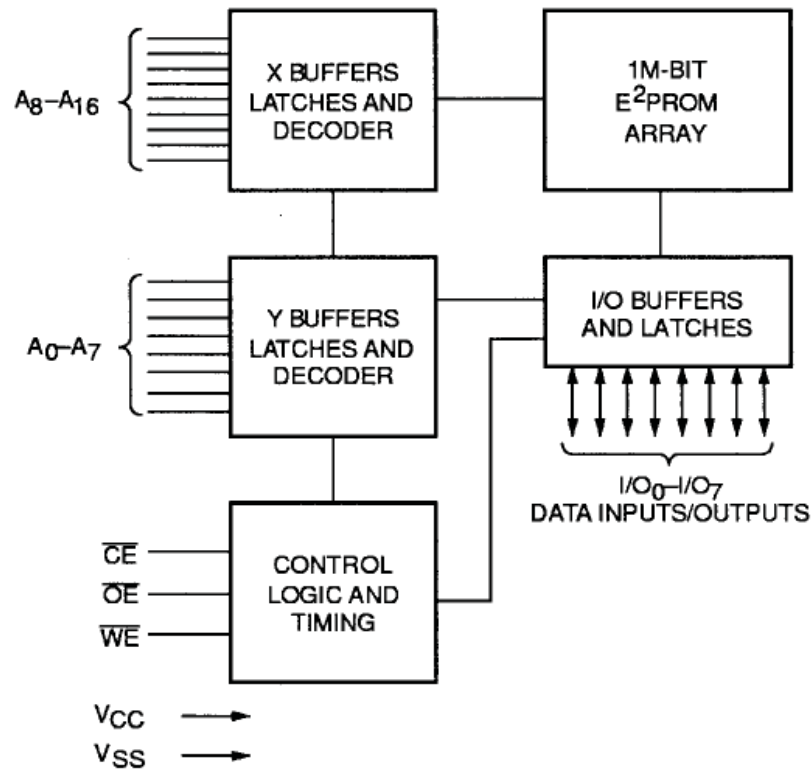
PIN ASSIGNMENT (Top View)			
32-Pin CFP (F), 32-Pin CerDIP (CW)			
NC	1	32	Vcc
A16	2	31	WE\
A15	3	30	NC
A12	4	29	A14
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE\
A2	10	23	A10
A1	11	22	CE\
A0	12	21	I/O 7
I/O 0	13	20	I/O 6
I/O 1	14	19	I/O 5
I/O 2	15	18	I/O 4
Vss	16	17	I/O 3

ware data protection is provided , in addition to noise protection on the WE signal and write inhibit during power on and off. Software data protection is implemented using JEDEC Optional Standard algorithm.

The AS28C010 is designed for high reliability in the most demanding applications. Data retention is specified for 100 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode and 10,000 cycles in the Byte Mode.

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## FUNCTIONAL BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### READ

Read operations are initiated by both OE\ and CE\ LOW. The read operation is terminated by either CE\ or OE\ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE\ or CE\ is HIGH.

### WRITE

Write operations are initiated when both CE\ and WE\ are LOW and OE\ is HIGH. The AS28C010 supports both a CE\ and WE\ controlled write cycle. That is, the address is latched by the falling edge of either CE\ or WE\, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE\ or WE\, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

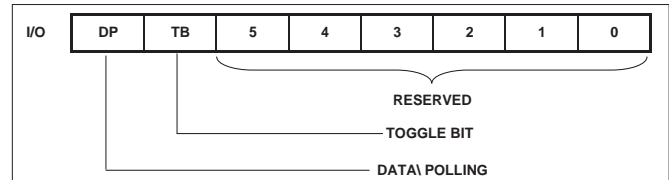
### PAGE WRITE

The page write feature of the AS28C010 allows the entire memory to be written in 5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the AS28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A<sub>8</sub> through A<sub>16</sub>) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty six bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE\ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding WE\. If a subsequent WE\ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

### WRITE

The AS28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.



### DATA\ POLLING

The AS28C010 features DATA\ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA\ Polling allows a simple bit test operation to determine the status of the AS28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data. Note: If the AS28C010 is in the protected state and an illegal write operation is attempted DATA\ Polling will not operate.

### TOGGLE BIT

The AS28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle, I/O<sub>6</sub> will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

Figure 1: Status Bit Assignment

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc Supply Relative to Vss.....-0.5V to +7.0V<sup>1</sup>  
 Voltage on any pin Relative to Vss.....-0.6V to +7.0V<sup>1</sup>  
 Storage Temperature .....-65°C to +150°C  
 Operating Temperature Range.....-55°C to +125°C  
 Soldering Temperature Range.....260°C  
 Maximum Junction Temperature\*\*.....+150°C  
 Power Dissipation.....1.0W

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*\* Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(-55°C ≤ T<sub>A</sub> ≤ 125°C; V<sub>CC</sub> = 5V ±10%)

PARAMETER	CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage <sup>1</sup>		V <sub>IH</sub>	2.0	V <sub>CC</sub> + 1.0V	V
Input Low (Logic 0) Voltage <sup>1</sup>		V <sub>IL</sub>	-1.0	0.8	V
Input Leakage Current	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	I <sub>LI</sub>		10	μA
Output Leakage Current	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub> , CE\=V <sub>IH</sub>	I <sub>LO</sub>		10	μA
Output High Voltage	I <sub>OH</sub> = -400 μA	V <sub>OH</sub>	2.4		V
Output Low Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>OL</sub>		0.4	V

Notes: 1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

PARAMETER	CONDITIONS	SYM	MAX				UNITS	NOTES
			-12	-15	-20	-25		
Power Supply Current: Operating	I <sub>OUT</sub> =0mA, V <sub>CC</sub> = 5.5V Cycle=MIN	I <sub>CC3</sub>	100	100	80	80	mA	
Power Supply Current: Standby	CE\=V <sub>CC</sub> , V <sub>CC</sub> = 5.5V	I <sub>CC1</sub>	500	500	500	500	μA	
	CE\=V <sub>IH</sub> , V <sub>CC</sub> = 5.5V	I <sub>CC2</sub>	3	3	3	3	mA	

## CAPACITANCE $T_A=+25^{\circ}\text{C}$ , $f=1\text{MHz}$ , $V_{CC}=5\text{V}$

PARAMETER	SYMBOL	MAX	UNITS	Test Conditions
Input Capacitance	$C_{IN}^{(2)}$	10	pF	$V_{IN}=0\text{V}$
Input / Output Capacitance	$C_{I/O}^{(2)}$	10	pF	$V_{I/O}=0\text{V}$

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(2)}$	Power-up to Read Operation	100	$\mu\text{s}$
$t_{PUW}^{(2)}$	Power-up to Write Operation	5	ms

## ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles Per Byte
Endurance	100,000		Cycles Per Page
Data Retention	100		Years

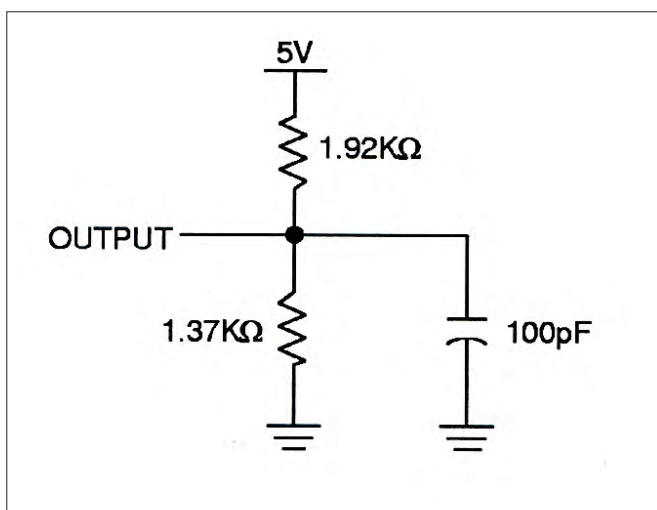
## MODE SELECTION

MODE	CE\	OE\	WE\	I/O
READ	$V_{IL}$	$V_{IL}$	$V_{IH}$	$D_{OUT}$
STANDBY	$V_{IH}$	X	X	High-Z
WRITE	$V_{IL}$	$V_{IH}$	$V_{IL}$	$D_{IN}$
DESELECT	$V_{IL}$	$V_{IH}$	$V_{IH}$	High-Z
WRITE INHIBIT	X	X	$V_{IH}$	---
	X	$V_{IL}$	X	---
DATA POLLING	$V_{IL}$	$V_{IL}$	$V_{IH}$	Data Out (I/O7)






## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

## EQUIVALENT A.C. LOAD CURRENT



## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Notes: (2) This parameter is periodically sampled and not 100% tested.

## AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $-55^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$ ;  $V_{CC} = 5\text{V} \pm 10\%$ )

### Test Conditions

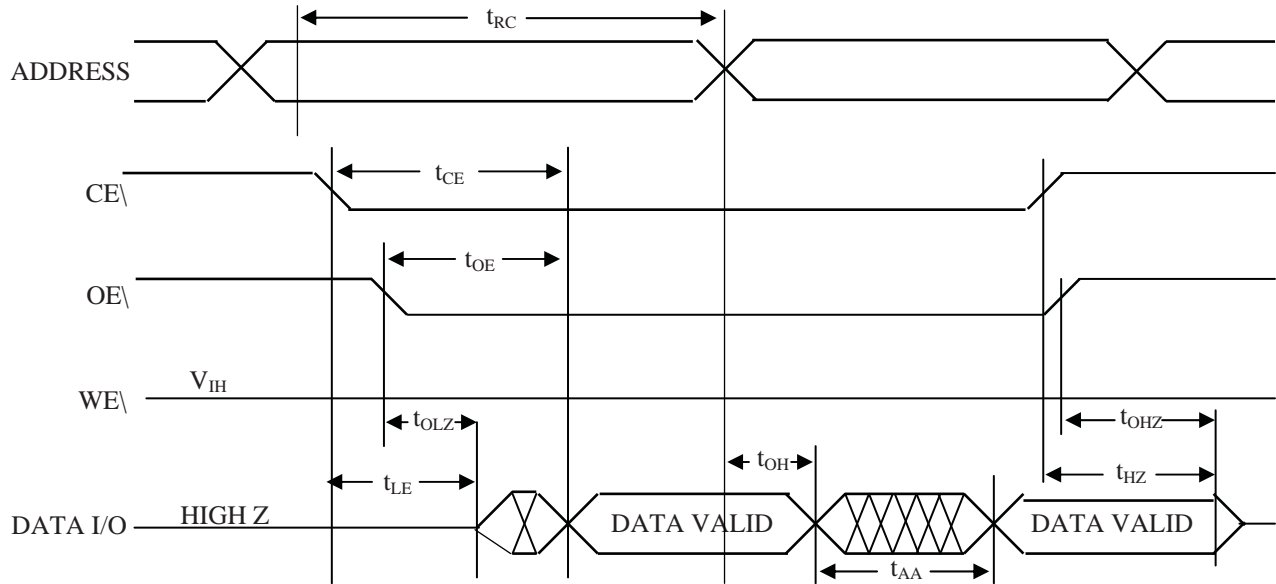
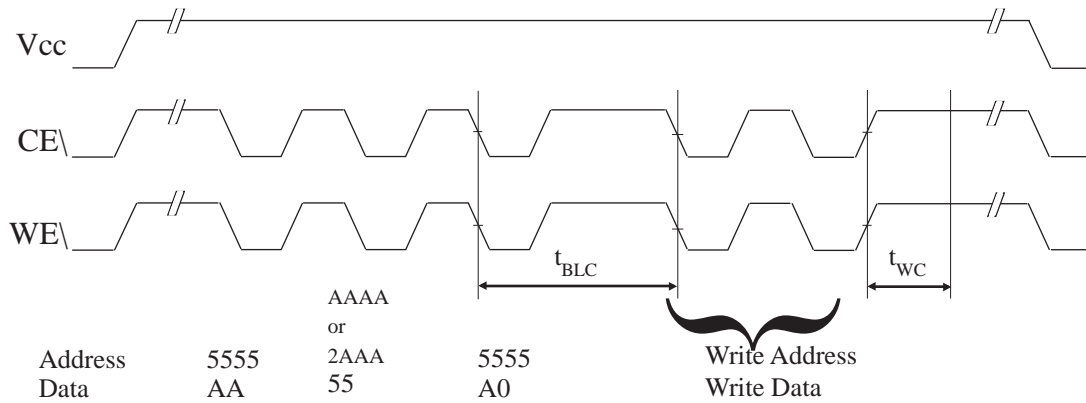
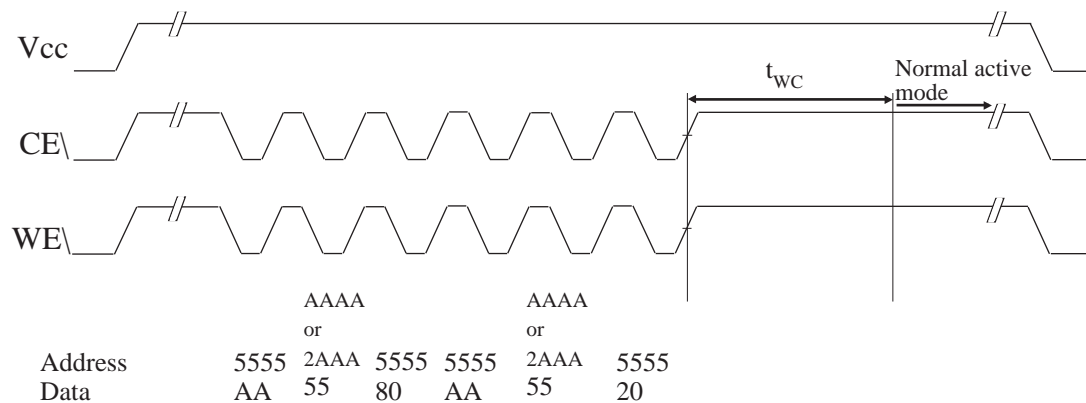
- Input Pulse Levels: 0.0V to 3.0V
- Input rise and fall times:  $\leq 20\text{ns}$
- Output Load: 1 TTL Gate +100pF (including scope and jig)
- Reference levels for measuring timing: 1.5V, 1.5V

Symbol	Parameter	-12		-15		-20		-25		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{RC}$	Read Cycle Time	120		150		200		250		ns
$t_{CE}$	Chip Enable Access Time		120		150		200		250	ns
$t_{AA}$	Address Access Time		120		150		200		250	ns
$t_{OE}$	Output Enable Access Time		50		50		50		50	ns
$t_{LZ}^{(3)}$	CE\ LOW to Active Output	0		0		0		0		ns
$t_{OLZ}^{(3)}$	OE\ LOW to Active Output	0		0		0		0		ns
$t_{HZ}^{(3)}$	CE\ HIGH to High Z Output		50		50		50		50	ns
$t_{OHZ}^{(3)}$	OE\ HIGH to High Z Output		50		50		50		50	ns
$t_{OH}$	Output Hold from Address Change	0		0		0		0		ns

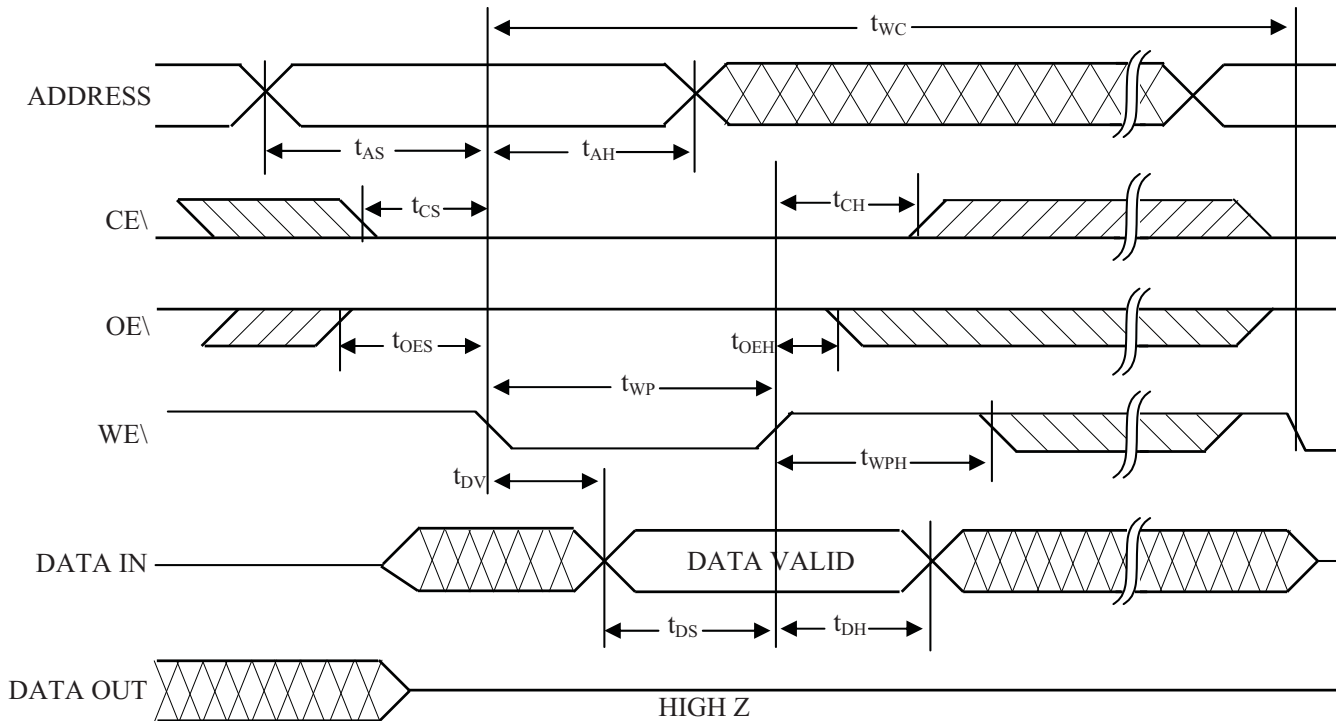
Notes: 3)  $t_{LZ}$  min.,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured, with  $C_L = 5\text{pF}$ , from the point when CE\ or OE\ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

## AC ELECTRICAL CHARACTERISTICS FOR WRITE OPERATIONS

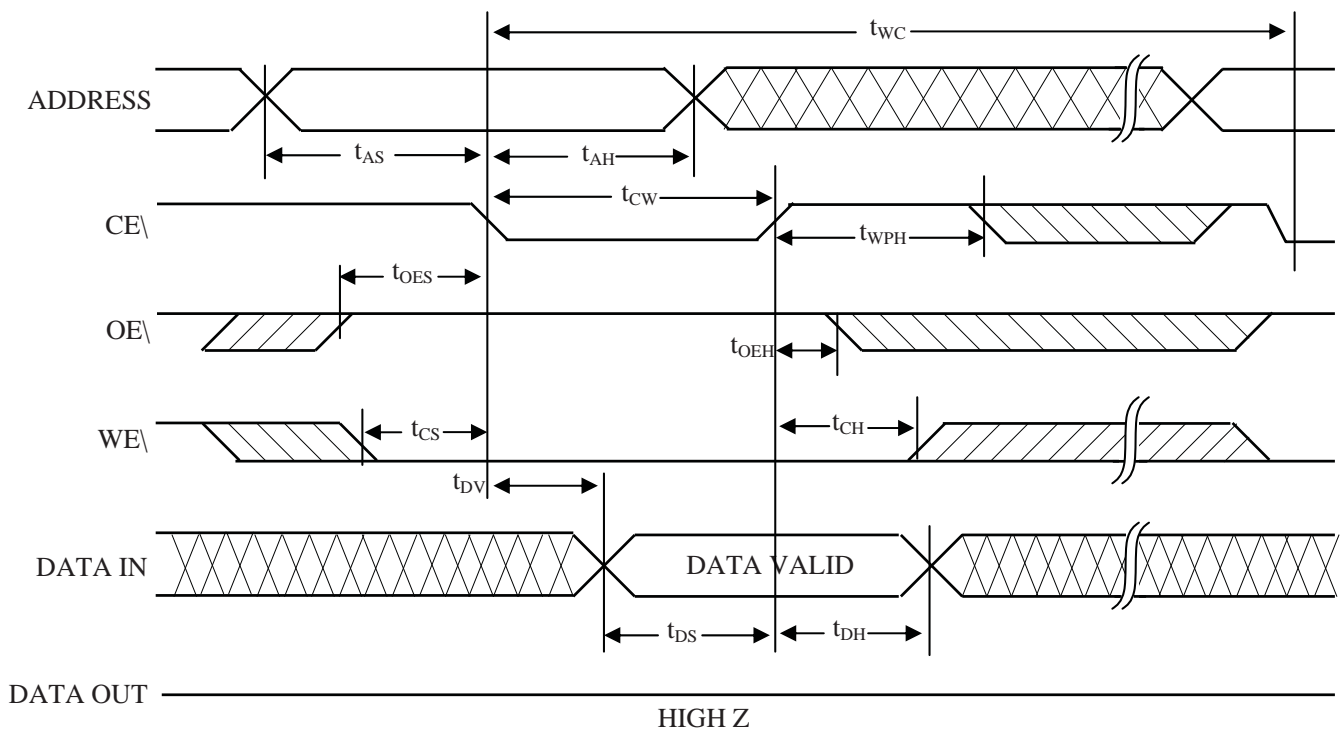
SYMBOL	PARAMETER	MIN	MAX	UNITS
$t_{WC}$	Write Cycle Time		10	ms
$t_{AS}$	Address Setup Time	0		ns
$t_{AH}$	Address Hold Time	50		ns
$t_{CS}$	Write Setup Time	0		ns
$t_{CH}$	Write Hold Time	0		ns
$t_{CW}$	CE\ Pulse Width	100		ns
$t_{OES}$	OE\ HIGH Setup Time	10		ns
$t_{OEH}$	OE\ HIGH Hold Time	10		ns
$t_{WP}$	WE\ Pulse Width	100		ns
$t_{WPH}$	WE\ HIGH Recovery	100		ns
$t_{DV}$	Data Valid		1	$\mu\text{s}$
$t_{DS}$	Data Setup	50		ns
$t_{DH}$	Data Hold	0		ns
$t_{DW}$	Delay to Next Write	10		$\mu\text{s}$
$t_{BLC}$	Byte Load Cycle	0.20	100	$\mu\text{s}$

**READ CYCLE**

**SOFTWARE DATA PROTECTION TIMING WAVEFORM (protection mode)**

**SOFTWARE DATA PROTECTION TIMING WAVEFORM (non-protection mode)**


### WE\ CONTROLLED WRITE CYCLE

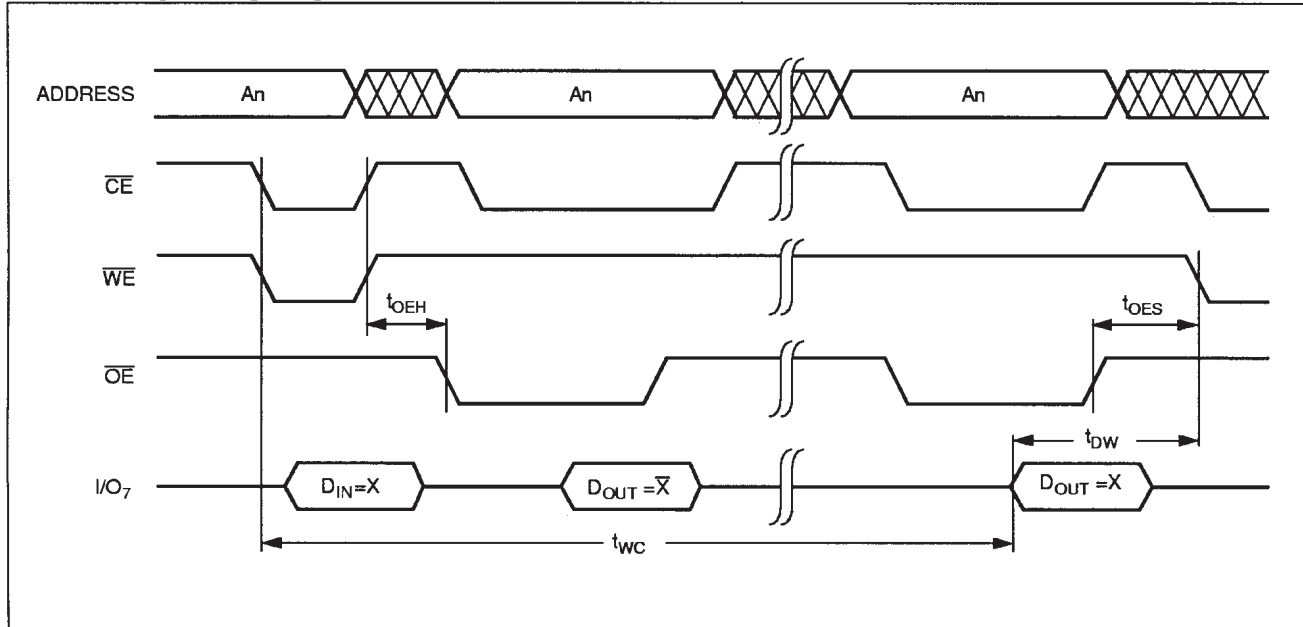


### CE\ CONTROLLED WRITE CYCLE

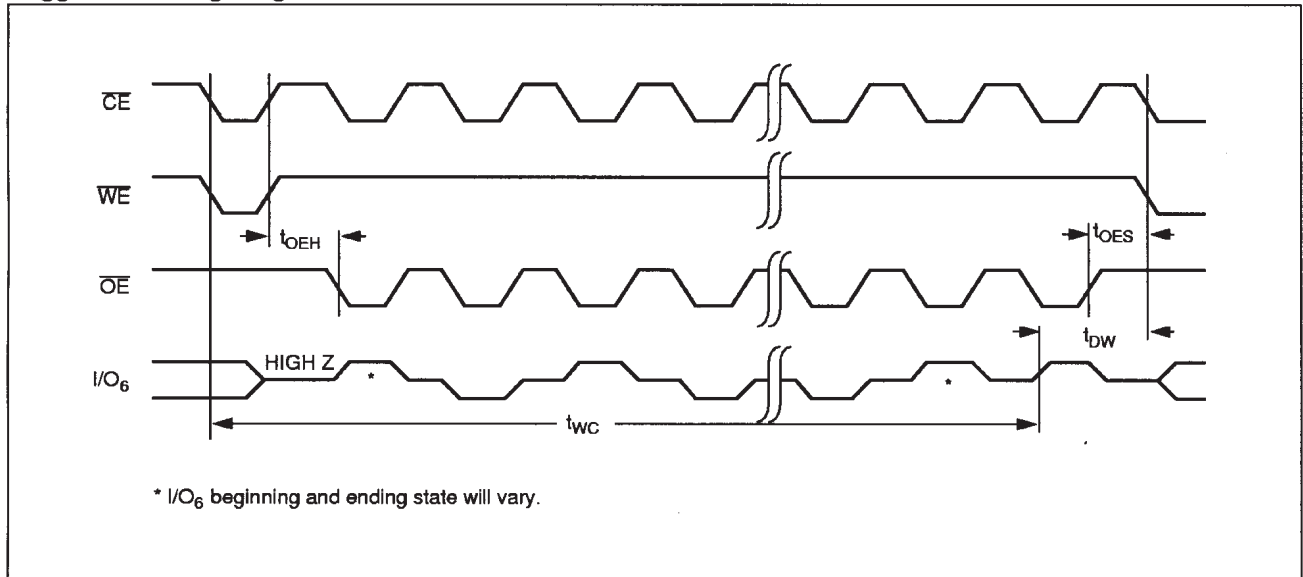




**DATA Polling Timing Diagram(7)**

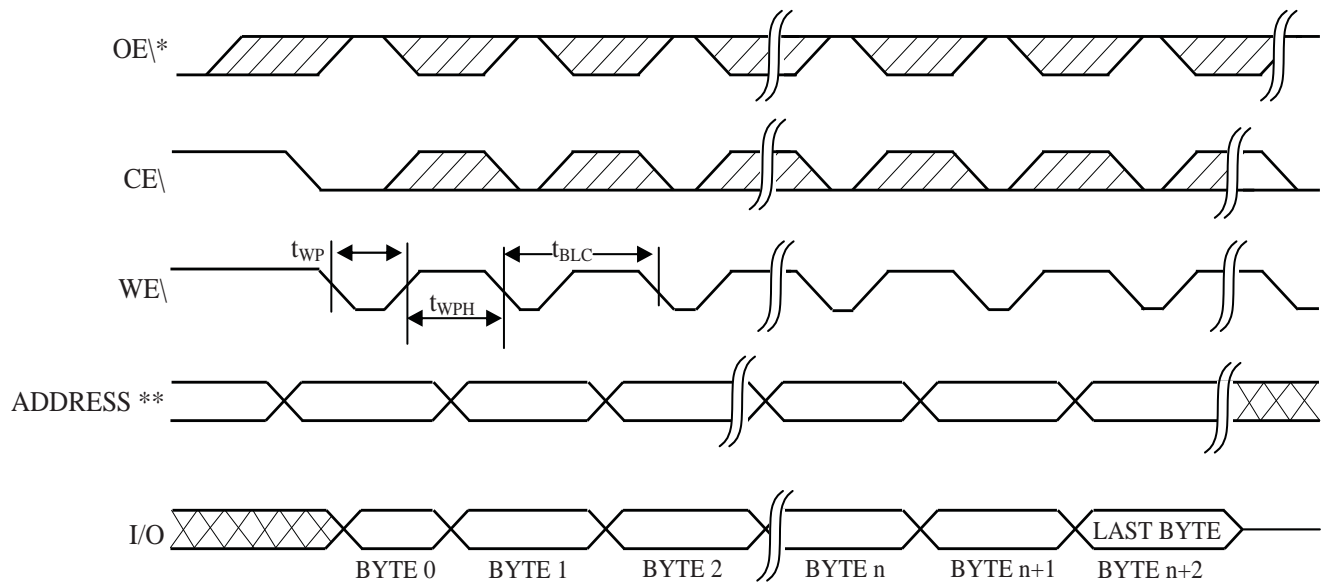


**Toggle Bit Timing Diagram**



**Notes:** (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

## PAGE WRITE CYCLE

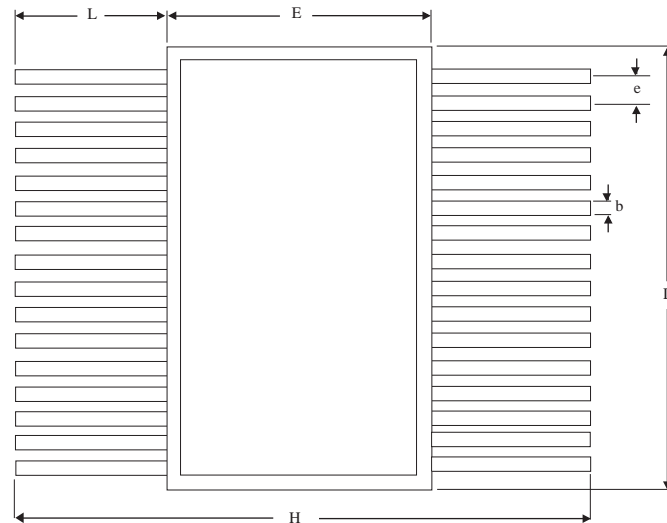


\* Between successive byte writes within a page write operation, OE $\setminus$  can be strobed LOW: e.g. this can be done with CE $\setminus$  and WE $\setminus$  HIGH to fetch data from another memory device within the system for the next write; or with WE $\setminus$  HIGH and CE $\setminus$  LOW effectively performing a polling operation.

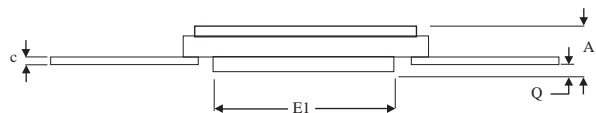
\*\* 1- For each successive write within the page write operation A<sub>8</sub>-A<sub>16</sub> should be the same or writes to an unknown address could occur.  
2- The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either CE $\setminus$  or WE $\setminus$  controlled write cycle timing.

## MECHANICAL DEFINITIONS\*

**Micros Case #306 (Package Designator F)  
SMD 5962-38267, Case Outline M**



**Top View**

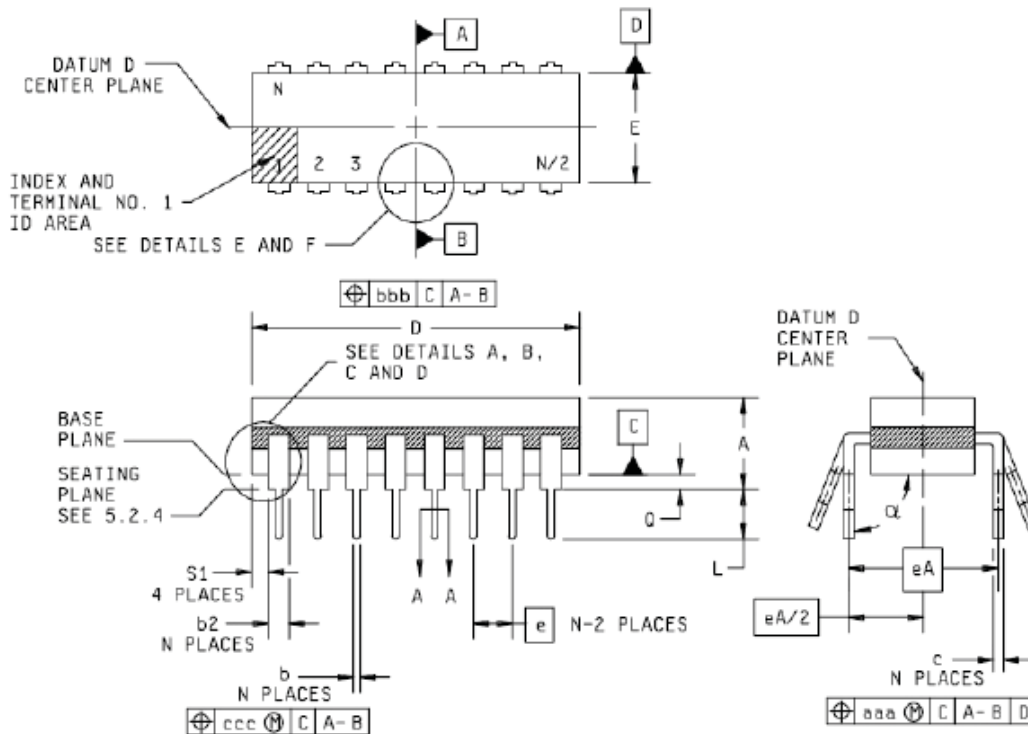


SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.097	0.123
A1	0.090	0.110
b	0.015	0.019
c	0.003	0.007
D	0.810	0.830
D2	0.745	0.755
E	0.425	0.445
E1	0.330	0.356
e	0.045	0.055
H	1.000	1.100
L	0.290	0.310
Q	0.026	0.037

**NOTE:** All drawings are per the SMD. Micross' package dimensional limits may differ, but they will be within the SMD limits.

\*All measurements are in inches.

### MECHANICAL DEFINITIONS\*



Symbol	Min	Max	Note	Symbol	Min	Max	Note
A	---	.225		eA/2	.300	BSC	
b	.014	.026	2	L	.125	.200	8
b1	.014	.023	3	Q	.015	.070	9
b2	.045	.065	4	S1	.005	---	10
b3	.023	.045	5	S2	.005	---	11
c	.008	.018	2	a	90°	105°	
c1	.008	.015	3	aaa	---	.015	
D	---	1.680	6	bbb	---	.030	
E	.510	.620	6	ccc	---	.010	
E2				M	---	.0015	2
E3				N		32	12
e	.100	BSC					
eA	.600	BSC					
Note	1,14						

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. The b2 minimum dimension of .045 inch (1.14 mm) was implemented 30 September 1992. Until that date, a minimum dimension of .038 (0.97 mm) was acceptable. See 5.2.4
5. Corner leads (1, N, N/2, and N/2+1) may be configured as shown in detail A. For this configuration dimension b3 replaces dimension b2.
6. This dimension allows for off-center lid, meniscus, and glass overrun.
8. Pointed or rounded lead tips as shown in details B and C are preferred to ease insertion, but are not mandatory.
9. Dimension Q shall be measured from the seating plane to the base plane.
10. Measure dimension S1 at all four corners, see 5.2.5.
11. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead
12. N is the maximum number of terminal positions.
14. See tables VI and VII for descriptive type designators.

\*All measurements are in inches.

## ORDERING INFORMATION

**EXAMPLE:** AS28C010CW-15/883C

Device Number	Package Type	Speed ns	Process
AS28C010	CW	-12	/*
AS28C010	CW	-15	/*
AS28C010	CW	-20	/*
AS28C010	CW	-25	/*

**EXAMPLE:** AS28C010F-15/883C

Device Number	Package Type	Speed ns	Process
AS28C010	F	-12	/*
AS28C010	F	-15	/*
AS28C010	F	-20	/*
AS28C010	F	-25	/*

### \*AVAILABLE PROCESSES

IT = Industrial Temperature Range      -40°C to +85°C  
 XT = Extended Temperature Range      -55°C to +125°C  
 Q= Full Military Processing              -55°C to +125°C

## MICROSS TO DSCC PART NUMBER CROSS REFERENCE\*

### Package Designator CW

<u>MICROSS Part #</u>	<u>SMD Part#</u>
AS28C010CW-25/Q	5962-3826701QXA
AS28C010CW-20/Q	5962-3826703QXA
AS28C010CW-15/Q	5962-3826705QXA
AS28C010CW-12/Q	5962-3826707QXA

### Package Designator F

<u>MICROSS Part #</u>	<u>SMD Part#</u>
AS28C010F-25/Q	5962-3826701QZA
AS28C010F-20/Q	5962-3826703QZA
AS28C010F-15/Q	5962-3826705QZA
AS28C010F-12/Q	5962-3826707QZA

\* ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.

**DOCUMENT TITLE**

128K x 8 EEPROM EEPROM Memory 5 Volt, Byte Alterable

**REVISION HISTORY**

<u>Rev #</u>	<u>History</u>	<u>Release Date</u>	<u>Status</u>
1.7	Corrected pin-out, page 1	January 2012	Release