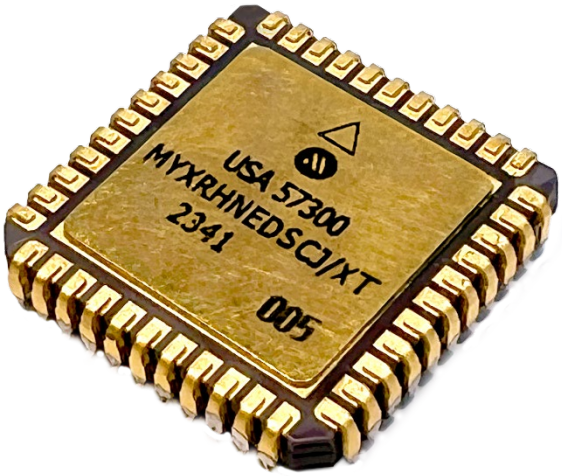
Standard-Performance NED

Nuclear Event Detector

Part Number: MYXRHNEDSCJ/XT, MYXRHNEDSCJ/H

Rad-Hard



Preliminary Data Sheet

Micross Standard-Performance Nuclear Event Detector (NED) features a 2X increase in radiation dose rate sensitivity and faster response times at 5X lower overdrive levels relative to legacy devices with integrated differential drivers providing SWaP reduction, improved noise immunity and reduced delay times. The Standard-Performance NED can be screened to XT (Extended Temperature, -55°C to 125°C) and MIL-PRF-38534 Class H and provides a greatly improved functional replacement for the nearly 40-year-old legacy NED solution.

Key Features

- Gamma Dose Rate Sensitivity Threshold Range Adjustable from 1 x 10^5 to 2 x 10^7 rads (Si) / sec.
- 44-Pin Hermetic J-Lead SMT Package (.650in x .650in x .113in)
- Integrated Differential Line Drivers and Receivers
- Radiation Specifications
  - Total Dose (Device Survivability): 1 x 10^6 rads(Si)
  - Dose Rate (Operate Through): 1 x 10^{12} rads(Si)/sec
  - Neutron Fluence (Device Survivability): 5 x 10^{13} neutrons/cm^2
- 3.3V Power Requirement
- -55°C to +125°C Temperature Range
- Integrated Differential Line Drivers and Receivers All Operate Through Promp
- t Dose without Extra Shielding

Benefits

- Low Minimum Dose Rate Sensitivity
- Fast Delay Time to Enable Rapid Shutdown and Minimize Damage to Other Electronics
- Rad-Hard for Strategic Environments
- Small Compact Package Facilitates Use on Densely Populated Circuit Cards and Boards
- Built-In Differential Drivers and Receivers Provide SWaP (Space, Weight & Power) Savings, Improved Noise Immunity, and Reduced Delay Times
- Use Output Signal to Shut Down Power Supplies, Take Processors Offline and Block Memory Write Operations

Applications

- Aircraft and Drones
- Defense Weapon Systems
- Satellites
- Military Ground Vehicles
- Nuclear Material Storage

Revision History

Revision	Description	Release Date
0.1	Initial Draft of Preliminary Datasheet	06/04/2025
1.0	Revised, including addition of application information	6/26/2025
1.1	Changed package type from non-hermetic to hermetic; Added reference to case ground pin; BIT pulse time; graphs for $R_{REF-ADJ}$ and C_{PULSE}; added mention about delay time test.	7/24/2025

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1.0 Description

Micross Standard-Performance Nuclear Event Detector (NED, Figure 1) provides an economical solution for detecting gamma radiation pulses from a nuclear event. For an overdrive ratio of just 2 (received radiation-to-dose rate threshold), the NED will assert its pulse and level differential output signals within 20ns following the leading edge of an incoming gamma radiation pulse. The NED's level output may then be reset by the assertion of a differential input signal. The MYXRHNEDSCJ/X features a minimum dose rate threshold of 1 x 10^5 rads(Si)/sec, thereby providing higher sensitivity than currently available NEDs. Users can increase the dose rate threshold upwards, to up to 2 x 10^7 rads(Si)/sec, by means of an external adjustment resistor. The Standard Performance NED, which is available in a hermetic 44-pin J-Lead ceramic package, is radiation hardened, enabling it to operate reliably in environments with high gamma doses and dose rates, neutrons and heavy ions; and provides immunity to latch up. It achieves this by using a rad-hard-by-design ASIC designed specifically for this purpose. Since the ASIC contains the line drivers and receivers on-board as Rad Hard blocks, no additional consideration is need for those functions.

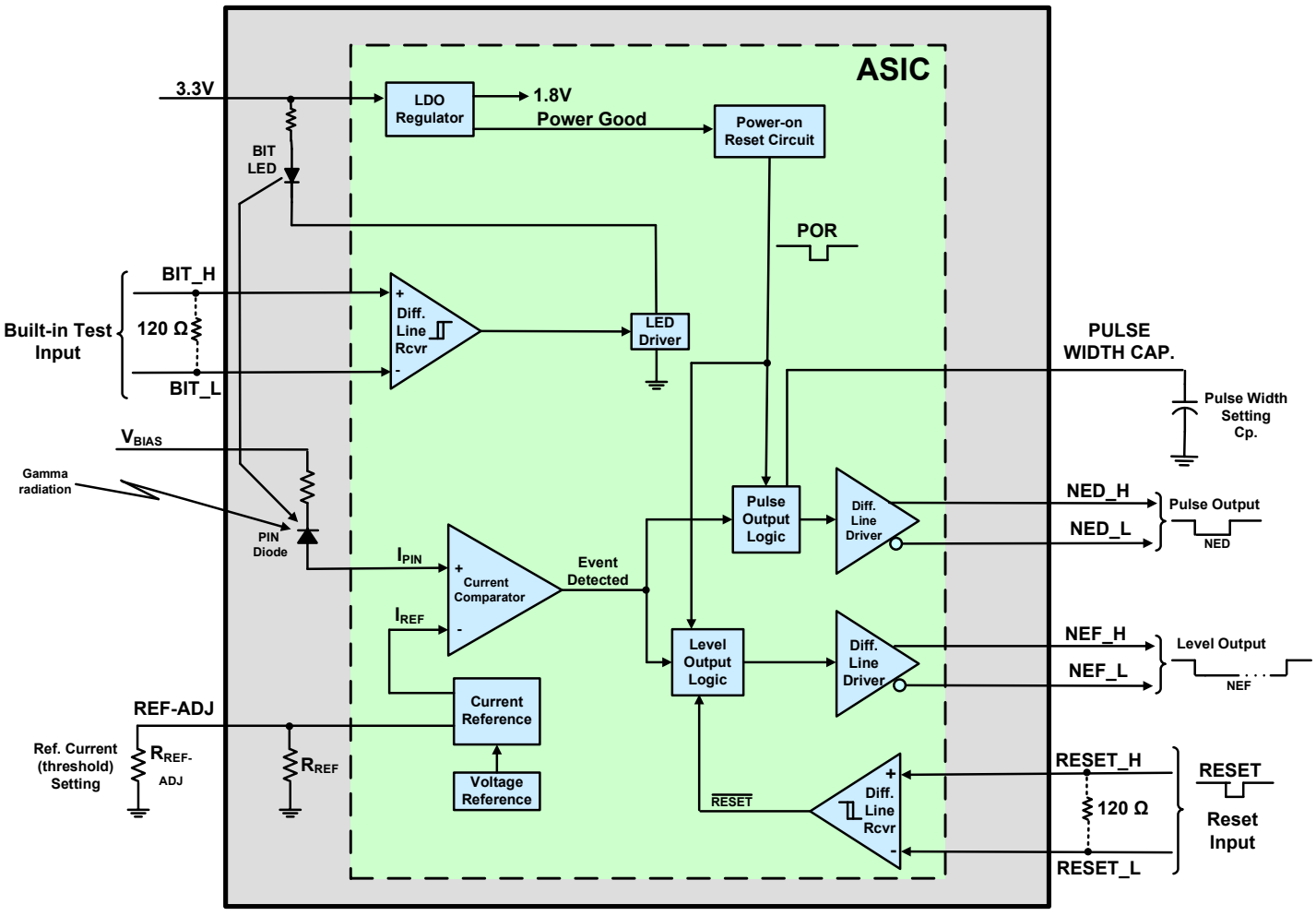

Figure 1. Nuclear Event Detector (NED) Block Diagram

2.0 Specifications

Table 1 provides the absolute maximum ratings for the MYXRHNEDHCJ/X nuclear event detector (NED), while Table 2 provides the electrical and mechanical specifications and characteristics.

Table 1. Absolute Maximum Range

Parameter	Min	Max	Unit
Hardened Supply Voltage	-0.5	3.6	V
PIN Diode Bias Voltage	0	100	V
Differential Receivers Line Voltage	-8.0	8.0	V
Differential Drivers Line Voltage	-0.5	3.6	V
ESD Sensitivity	Class 2		
Junction Temperature, TJ	-55	150	°C
Storage Temperature Range	-65	150	°C
Total Dose (Device Survivability)		1×10^{6}	rads(Si)
Dose Rate (Operate Through)		1×10^{12}	rads(Si)/sec
Neutron Fluence (Device Survivability)		5×10^{13}	neutrons/cm^2
SEE LET Threshold		40	MeV-cm^2/g

Table 2. Electrical Specs and Characterisitics

Parameter	Symbol	Conditions	Min	Max	Unit	Group A Subgroups
Approximate Dose Rate Detection Range		V_{BIAS} = 20 volts, Adjustable by External Resistor	5×10^{4}	2×10^{7}	Rads(Si)/sec	
Dose Rate Threshold Variation Over Temperature		Relative to Room Temperature Threshold Over Temperature Range	-20	+20	%	
Hardened Power Supply Operational Voltage	V_{CC}		3.0	3.6	V	1,2,3
Hardened Power Supply Current		Notes 1,2				
Both differential driver output circuits unterminated	I_{CC}	V_{CC} = 3.3V		5	mA	1,2,3
One differential driver output circuit terminated				35		
Both differential driver output circuits terminated				65		
PIN Diode Bias Voltage	V_{BIAS}		4.5	100	V	1,2,3
PIN Diode Bias Current Standby	I_{BIAS}			10	µA	1,2,3

Table 2. Electrical Specs and Characteristics Cont.						
Parameter	**Symbol**	**Conditions**	**Min**	**Max**	**Unit**	**Group A Subgroups**
Radiation Propagation Delay Time Gamma Dose Rate = 2 x 10^5 rads(Si)/second Gamma Dose Rate = 2 x 10^7 rads(Si)/second	t_D	Notes 3,4 V_{BIAS} = 20 Volts		20 12	ns	
Differential Receivers' Voltage Threshold	V_{DR}	V_{CC} = 3.3V	-0.2	0.2	V_{PK}	1,2,3
Differential Receivers' Common Mode Voltage Range	V_{CM}	V_{CC} = 3.3V	-7.0	7.0	V	1,2,3
Differential Receivers' Hysteresis Voltage	$V_{RX-HYST}$	V_{CC} = 3.3V	50 typ.		mV	1,2,3
Differential Line Driver Differential Output Voltage	V_{DT}	V_{CC} = 3.3V	3.0	10.0	$V_{PK-to-PK}$	1,2,3
Pulse Output Pulse Width Range	t_{PULSE}	Adjustable by External Capacitor	0.1	10	ms	
RESET Pulse Width	t_{RESET}		250		ns	9,10,11
BIT Pulse Width	t_{BIT}		10		µs	
Operating Temperature Range	$T_{OPERATION}$		-55	+125	°C	
Package Options			Plastic and Ceramic BGA			
Outline Dimensions			17.11 x 17.55 x 3.05 typ. (0.691 x 0.691 x 0.12) typ.		mm (in)	
Mass (Weight) Plastic BGA Ceramic BGA			 0.2 typ. (0.007 typ.) 0.5 typ. (0.018 typ.)		 g (oz) g (oz)	
Lot Qualification and Acceptance Testing			In accordance with MIL-PRF-38534 Class H			

Notes:

1. The maximum values for I_{CC} assume the dose rate threshold is set to its minimum value of 5 x 10^4 rads(Si)/sec. For the external adjustment threshold resistor selected for the maximum dose rate threshold of 2 x 10^7 rads(Si)/sec, the max. value of I_{CC} increases by 7 mA. Refer to section 3.5.
2. For the NED and NEF line drivers, the termination loads on the line drivers are assumed to be 120 ohms differential (resistive). The use of terminations with series capacitors will reduce power dissipation accordingly.
3. Dose rate threshold is set to its minimum value of 1 x 10^5 rads(Si)/sec.
4. Delay time t_D is defined as the time from the 50% point of the rising edge of the incoming gamma radiation pulse to the 50% point of the high-to-low voltage transition for the NED and NEF differential output signals.

3.0 Operation

3.1 ASIC-Based Design

Micross' ASIC-based design provides multiple benefits relative to legacy nuclear event detectors:

1. It enables construction of a NED in a smaller and lighter package, capable of surviving prompt dose radiation.
2. Inclusion of differential drivers on chip improves overall response time, while legacy products suffer further response time degradation when external drivers are added.
3. By greatly reducing the number of components, wire bonds and interconnects, the Micross NEDs' reliability (MTBF) will be significantly higher than that of other NEDs.
4. Use of sub-micron ASIC technology and operation from lower power supply voltages will reduce the NED's power consumption and dissipation.
5. As a means of mitigating against obsolescence, Micross is not dependent on third-party suppliers for key components.
6. Micross' selected trusted foundry is on-shore and offers a 180 nm process with the capability to produce chips that meet the NED's radiation requirements. These requirements are:
   - Total gamma dose: 300 krads (Si), with a goal of 1 Mrads(Si)
   - Gamma dose rate (operate-through): 1 x 10^{12} rads(Si)/sec
   - Neutron fluence: 10^{13} n/cm^2

3.2 Functional Overview

As shown in Figure 1, the MYXRHNEDSCJ/X NED includes a 3.3V-to-1.8V LDO regulator. With the exception of the PIN diode and the two differential line drivers, all circuitry in the NED is powered by this on-ASIC's 1.8V supply rail. The two differential line drivers are powered directly by the 3.3V input power.

The NED includes a PIN diode to sense incoming gamma radiation from a nuclear explosion. Gamma radiation will result in current flowing through the reverse-biased PIN diode into the "+" side of a current comparator.

The input to the "-" side of the current comparator is provided by a reference circuit. This reference current is user-adjustable by means of the external resistor $R_{REF-ADJ}$ (see Figure 1 and section 3.8). As explained in section 3.5, installing a lower value for $R_{REF-ADJ}$ will increase the value of the reference current and as a result, increase the value of the NED's dose rate threshold.

When the PIN diode current exceeds the reference current, the output state of the comparator will assert active, thereby indicating that a nuclear event has been detected.

Following power turn-on, when the 1.8V regulator senses that its output has exceeded a voltage of approximately 1.0 volt, it will assert its POWER GOOD output signal. This will result in the generation of a negative-going "POR" (power-on reset) pulse. This pulse will reset the NED's two differential outputs NED and NEF to their quiescent (inactive) states of logic "1". Once this occurs, the NED and NEF differential outputs will remain in their de-asserted states (high) until a nuclear event is detected.

Following the detection of a nuclear event, NED and NEF will transition from their quiescent, de-asserted states of logic "1" (high) to their active, asserted states of logic "0" (low). The NED output will assert low for a fixed

amount of time, as determined by the value of an external capacitor (see Figure 1). The NEF (Flag) output will remain asserted until the receipt of a negative going pulse on the RESET differential input. A logic "0" pulse on the RESET input of 250 ns or more will clear the NEF output back to its de-asserted state.

3.3 PIN Diode

Similar to most existing NED designs, the sensing element in Micross' Nuclear Event Detector is a PIN diode. Most commercially available PIN diodes targeted to sensing applications are designed to operate at longer wavelengths, such as RF, visible, infrared, ultraviolet and X-ray. In particular, they're not designed to be optimized for detecting gamma radiation. For use in its NED, Micross has designed and fabricated its own PIN diode that's optimized for detecting gamma radiation. This internal development and captive manufacturing will ensure Micross with a reliable supply of PIN diodes, providing very strong mitigation against future obsolescence.

During its PIN diode development, Micross Components focused on the goals of wide dynamic range and fast response time in response to short duration pulses of gamma radiation. The PIN diode development involved extensive testing and characterization of the PIN diode in a flash X-ray facility.

To provide a reverse bias voltage to the NED's PIN diode, it's highly recommended to apply a minimum voltage of +15V to the PIN_Diode_Bias input (V_{BIAS}). Although it's possible to operate the NED from a lower value of V_{BIAS}, this will reduce the NED's sensitivity and therefore increase its dose rate threshold. It's also possible to reduce the NED's minimum dose threshold level and response time to a nuclear event by increasing the value of this voltage above 15V.

In the case of a nuclear event, the PIN diode current can spike to very high levels depending on the radiation level. To provide protection, the NED includes a 2.5 kΩ current-limiting resistor in series with the PIN diode. For a worst-case scenario and assuming V_{BIAS} = 15V, the maximum reverse bias current that would flow through the NED = 15V/ 2.5 kΩ = 6 mA.

3.4 Detector Circuit

In addition to the PIN diode, the most critical functional block of the NED is its detector circuit. For this function, Micross designed a current comparator circuit in its NED ASIC. In contrast to the voltage comparator used in legacy NEDs, Micross' use of a current comparator provides better speed performance by minimizing the impedance seen by the detector. This minimizes the value and effect of the circuit's inherent RC time constant.

The detector circuit includes a reference current circuit. The reference circuit provides a DC current output based on the input from a precision voltage source. To allow users to set the value of the NED's dose rate threshold, the reference current and therefore the dose rate threshold is programmable by means of an external resistor. The reference current circuit includes temperature compensation to offset temperature-dependent variations in the PIN diode and the current comparator. One of the goals for the detector's current comparator circuit is to provide very fast detection speed that's largely independent of the NED's threshold sensitivity setting.

Based on the use of a custom PIN diode and the inherent advantages of a current comparator, the MYXRHNEDSCJ/X provides superior performance for minimum dose rate threshold and delay time performance. The MYXRHNEDSCJ/X provides a minimum dose rate threshold of to 1 x 10^5 rads(Si)/sec or lower. The major

benefit of this is to detect the fast-rising edge of the nuclear event sooner and to reduce the number of false negative indications.

Relative to other NEDs, for a programmed gamma dose rate threshold of 1 x 10^5 rads/sec and detected gamma dose rate of 2 x 10^5 rads/sec (overdrive ratio = 2), the MYXRHNEDSCJ/X also provides a significant improvement relative to other NEDs for the total delay time between the leading edge of a gamma radiation pulse and the assertion of its differential output signal. The MYXRHNEDSCJ/X reduces the value of this total internal delay time to 20 ns for an overdrive ratio of 2. Other NEDs require an overdrive ratio of ten to provide the same delay time performance. For users, NED delay time is a critical parameter, since shorter delays enable improved protection of other on-board electronic circuitry.

3.5 Variable Dose Rate Threshold

As shown in Figure 1, the NED provides a means to program the value of its dose rate threshold. This is done by connecting a resistor designated as $R_{REF-ADJ}$ between the signal $R_{REF-ADJ}$ and GROUND. If no resistor is connected between R_{EF-ADJ} and GROUND, the dose rate threshold defaults to its minimum value of approximately 5 x 10^4 rad(Si)/sec. To configure the NED for a higher value of dose rate threshold, it's necessary to connect an external resistor between $R_{REF-ADJ}$ and GROUND.

To program for a value of dose rate threshold = DRT, the value of the external resistor is computed as follows:

R_0 is the parallel combination of an internal 9,592 ohm internal resistor and the external user-selectable resistor $R_{REF-ADJ}$.

$$R_0 = \frac{2.9 \cdot 10^9}{DRT^{1.0961}}$$

The value of the external user-selectable resistor is computed as follows:

$$R_{REF-ADJ} = \frac{9{,}592 \cdot R0}{(9{,}592 - R0)}$$

For example, to configure the NED for a dose rate threshold of 1 x 10^6 rad(Si)/sec, the value of the external resistor is computed as follows:

For DRT = 10^6, $R_0 = \frac{2.9 \cdot 10^9}{(1 \cdot 10^6)^{1.0961}} =$ 769 ohms

$R_{REF-ADJ} = \left(\frac{9{,}592 \cdot 769}{9{,}592 - 769}\right) =$ 836 ohms

The graph of Figure 2 shows the relationship between dose rate threshold and the value of the adjustment resistor.

3.6 Differential Line Drivers and Receivers

As shown in Figure 1, the MYXRHNEDSCJ/X includes differential line drivers and receivers for the various digital output and input signals. It includes differential drivers for the NED pulse output and NEF level output, and differential receivers for the RESET and BIT input signals.

Differential drivers and receivers provide improved signal integrity, noise rejection and common mode rejection relative to single-ended divers and receivers, especially single-ended drivers consisting of open-collector or

open-drain circuits. Micross designed the differential drivers and receivers to provide reliable operation in the presence of the types of noise transients that occur during nearby nuclear events. To lessen the effects of noise, the receivers include built-in circuit protection, hysteresis and common mode rejection. The NED's differential drivers and receivers are designed to meet or exceed the requirements of the EIA RS-422 standard. For the transmitter outputs, this will include a minimum differential output voltage of 3.0 volts peak-to-peak.

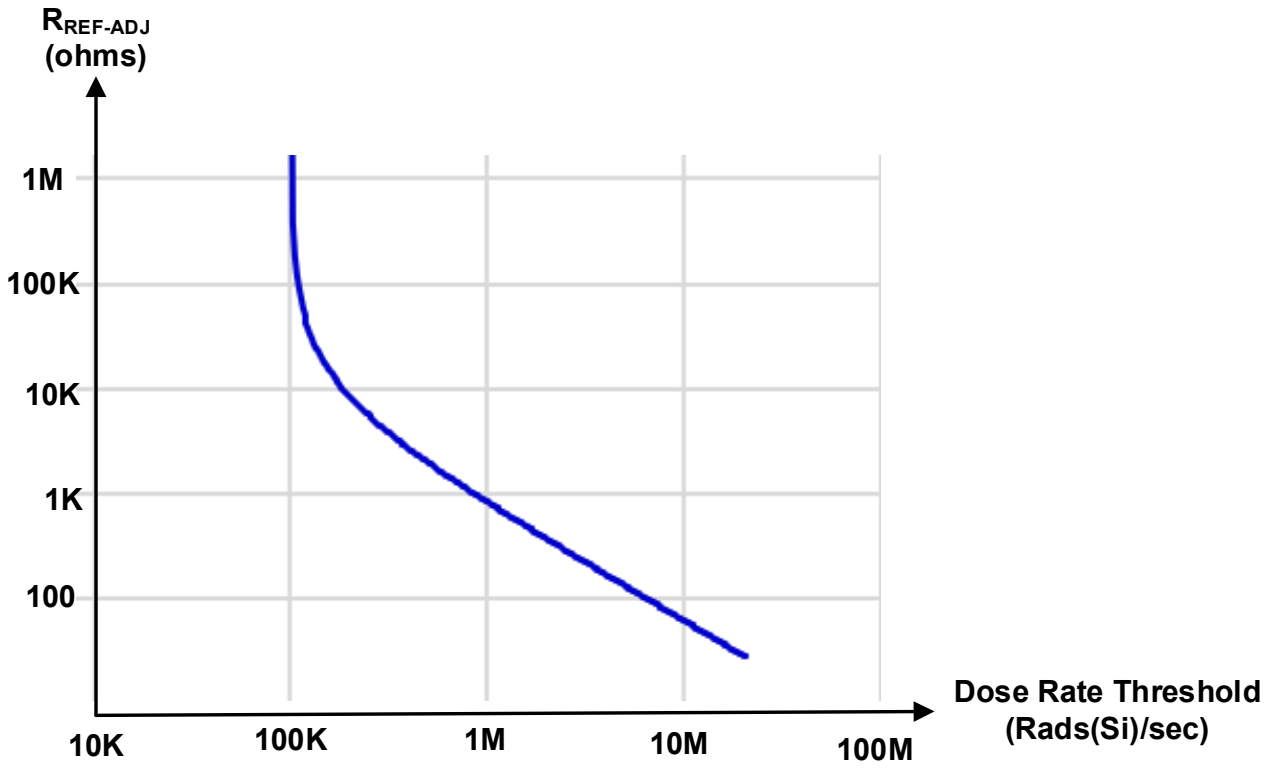

Figure 2. Dose Rate Threshold Adjustment Resistor

The differential receiver for the RESET input will be biased to provide a logic "1" (inactive) output when there's no incoming signal, while the differential receiver for the BIT (Built-in Test) input will be biased to provide a logic "0" (inactive) output when there's no incoming signal. In addition, the differential receivers will include positive and negative threshold voltages of less than ±0.2 V peak, provide a minimum hysteresis voltage of 50 mV and operate with common mode voltages equal to or greater than the range of -7V to +7V.

The external signals for the differential and single-ended line drivers and receivers will include clamping diodes to VCC and GROUND to protect against electrostatic discharge (ESD).

The delays through the MYXRHNEDSCJ/X's on-ASIC differential line drivers are approximately 5 ns. Note that other NEDs provide single-ended open-collector drivers rather than differential drivers. In order to gain the benefit of differential signaling using these NEDs, it's necessary to use external differential drivers. For the MYXRHNEDSCJ/X, the inclusion of the internal differential drivers provides a large improvement over the use of external drivers, which add additional delays of approximately 15 ns.

To ensure reliable operation of the NED_H and NED_L differential pulse type output and/or the NEF_H and NEF_L differential level type output, it's necessary to terminate the end of the differential cable going into a differential receiving circuit with a resistor that matches the cable's differential characteristic impedance. For signals adhering to the RS-422 standard, the standard value for the cable characteristic impedance and terminating resistance is 120 ohms.

3.7 Differential and Single-Ended Operation

The NED's BIT and RESET inputs, and NED and NEF outputs can be operated as either differential pairs or as single-ended signals. As shown in Figure 1, to operate the BIT and/or RESET inputs in differential mode, it is recommended to connect a 120 ohm termination resistor between BIT_H and BIT_L or between RESET_H and RESET_L. To operate these inputs in single-ended mode, it is recommended to connect a termination resistor between the used input signal (e.g., BIT_H) and GROUND and to connect the unused input (e.g., BIT_L) to a voltage of approximately 0.5* V_{DD} through a simple resistive voltage divider.

Similarly, the NED's NED and NEF output signals can also be operated as either differential pairs or as single-ended signals. When operating NED_H and NED_L and/or NEF_H and NED_L in differential mode, it is recommended to connect a termination resistor across the receiving end of the differential link. The value of this resistor should match the characteristic impedance of the interconnecting cable. For RS-422 type signals, cables with 120ohm impedance are commonly used. To use these output signals in single-ended mode, it is recommended to connect a termination resistor (e.g., 120 ohms) between the used signal conductor (e.g., NED_H) and GROUND at the receiving end of the signal link.

3.8 NED_H/NED_L Pulse Width Setting

To program the pulse width duration from the NED_DET_H/NED_DET_L differential output, connect a capacitor between the signal Pulse Width Cap. and ground. The value of this capacitor should be:

$$\text{Cap value} = \frac{\text{Pulse (sec)}}{16{,}000}$$

For example, for a pulse width = 100 µs,

$$\text{Cap value} = \frac{0.0001}{16{,}000} = 6.25 \text{ nF}$$

The graph of Figure 3 shows the relationship between desired output pulse width and the value of the capacitor.

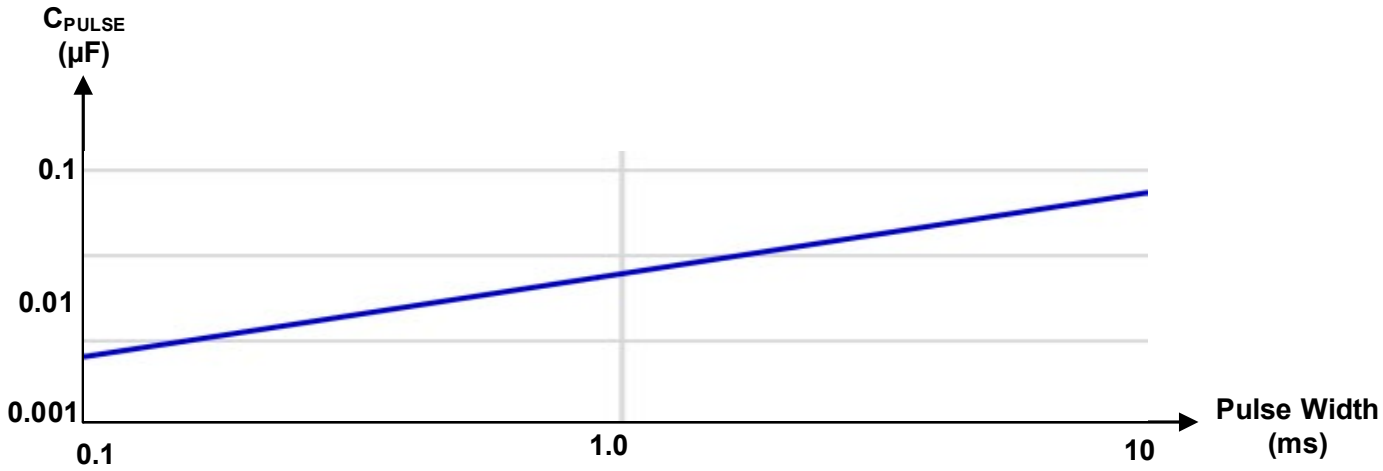

Figure 3. Pulse Width Capacitor

3.9 Built-In Self-Test

To enable Built-in self-test (BIT), the MYXRHNEDSCJ/X includes an LED. This LED will be controlled by the BIT (built-in test) input signal. When BIT is asserted to logic "1", the LED will illuminate the PIN diode. During this test, if the Event Detected signal asserts high, the self-test will be considered to have passed and the NED's output signal will assert active. However, if the NED and NEF signals remain inactive, the self-test will have failed. To ensure that the NED_DET pulse output and NED_FLG latched level output assert during self-test, the differential BIT signal should be asserted for at least 10 µs.

3.10 Pinout and Signal Descriptions

Table 3 provides the pinout and signal descriptions for the NED.

Table 3. Signal Pinout and Descriptions

Pin Number	Signal Name	Input or Output	Description
1	N/C	--	
2	GROUND	--	GROUND
3	GROUND	--	GROUND
4	NED_DET_H	Output	NED differential pulse output. Quiescently, NED_DET_H outputs a high level and NED_DET_L outputs a low level. When the NED detects a nuclear event, NED_DET_H transitions to a low level and NED_DET_L transitions to a high level for the programmed duration of the pulse output. The length of the pulse is determined by the value of the external pulse width control capacitor connected between pin 14 and GROUND.
5	NED_DET_L	Output	
6	N/C	--	

Table 3. Signal Pinout and Descriptions			
Pin Number	**Signal Name**	**Input or Output**	**Description**
7	GROUND	--	GROUND
8	GROUND	--	GROUND
9	N/C	--	
10	V_{DD}	Input	3.3V power input
11	V_{DD}	Input	3.3V power input
12	V_{DD}	Input	3.3V power input
13	N/C	--	
14	Pulse Width Cap.	--	As described in section 3.8, the duration of the NED's pulse type output asserted by the differential pair NED_DET_H and NED_DET_L needs to be configured by connecting a capacitor between Pulse Width Cap. and GROUND.
15	N/C	--	
16	N/C	--	
17	POR_cap	--	This pin may be left unconnected. However, it may be used to increase the NED's power-on reset time. To do that, connect an external capacitor between POR_cap and GROUND.
18	GROUND	--	GROUND
19	N/C	--	
20	N/C	--	
21	GROUND	--	GROUND
22	$R_{REF-ADJ}$	--	External resistor to adjust the NED dose rate threshold. To configure the NED for its minimum dose rate threshold of 5×10^4 rad(Si)/sec, this pin should be left open. As described in section =, the NED's dose rate threshold can be adjusted to a higher value by connecting a resistor between $R_{REF-ADJ}$ and GROUND.
23	N/C	--	
24	BIT-H	Input	Differential Built-in Test (BIT) input. To perform the NED's built-in test, this signal should be asserted with BIT-H driven high relative to BIT-L. To determine if the NED has passed its built-in test, verify that the NEDA_DET_H(L) pulses for the period programmed by the Pulse Width Cap. and that NEDA_FLG_L asserts its latched level output until NED_RST_H(L) is asserted. To ensure that the NED_DET pulse and NED_FLG latched outputs assert during self-test, the differential BIT signal should be asserted for at least 10 µs.
25	BIT-L	Input	
26	N/C	--	

Table 3. Signal Pinout and Descriptions			
Pin Number	**Signal Name**	**Input or Output**	**Description**
27	NED_RST_H	Input	Differential NED Reset input. For normal operation, NED_RST_H should be asserted high and NED_RST_L should be asserted low. Following detection of a nuclear event, the NED_FLG_H(L) latched differential level output will assert. To clear the NED_FLG_H(L) output, it's necessary to assert NED_RST_H(L). This is done by driving NED_RST_H low and NED_RST_L high for a minimum of 250ns.
28	NED_RST_L	Input	
29	1.8V	Input	Internal 1.8V output. No connection necessary.
30	N/C	--	
31	N/C	--	
32	GROUND	--	GROUND
33	GROUND	--	GROUND
34	N/C	--	
35	PIN_Diode_Bias	Input	PIN Diode Bias. To provide a reverse bias voltage to the NED's PIN diode, it's necessary to apply a minimum voltage of +15V to the PIN_Diode_Bias input. It's possible to reduce the NED's response time to a nuclear event by increasing the value of this voltage.
36	N/C	--	N/C
37	N/C	--	N/C
38	Case Ground	--	Case ground. It is recommended to connect this pin to chassis ground.
39	N/C	--	N/C
40	N/C	--	N/C
41	N/C	--	N/C
42	N/C	--	N/C
43	NED_FLG_H	Output	NED latched flag differential output. Quiescently, NED_FLG_H outputs a high level and NED_FLGT_L outputs a low level. When the NED detects a nuclear event, NED_FLG_H transitions to a low level and NED_FLG_L transitions to a high level. The state of this differential output signal is internally latched and the output remains asserted until the NED_RST_H(L) input is asserted by driving NED_RST_H low and NED_RST_L high for a minimum of 250 ns.
44	NED_FLG_L		

4.0 Application Information

4.1 Input Signals

The NED includes two pairs of differential input signals: the NED_RST_H and NED_RST_L RESET inputs for resetting the flag (level type) output signal and the BIT-H and BIT-H inputs for activating built-in test. These signals may be operated as either differential pairs or as single-ended signals.

4.1.1 Differential Inputs

For operating the RESET and BIT signals as differential pairs, the signal pairs should be terminated with 120 ohm resistors as shown in Figure 4. To reduce power dissipation by the differential drivers from an external circuit, it's recommended to include a capacitor (C_{TERM}) in series with the termination resistor, as shown in Figure 4(b). This prevents the need for the driving circuit to provide current except during signal transitions between its high and low states. To minimize reflections, it's recommended that the RC time constant of the series RC termination be approximately equal to or greater than the anticipated pulse width.

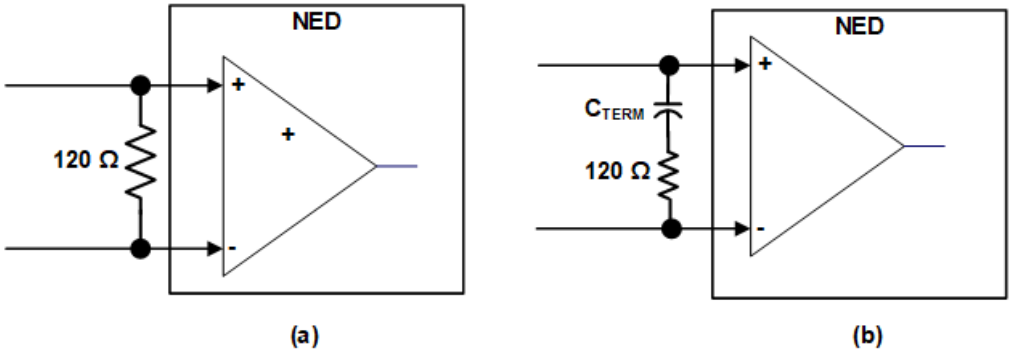

Figure 4. Differential Input Signal Termination
(a) Simple Termination; (b) AC-Coupled Termination

4.1.2 Single Ended Inputs

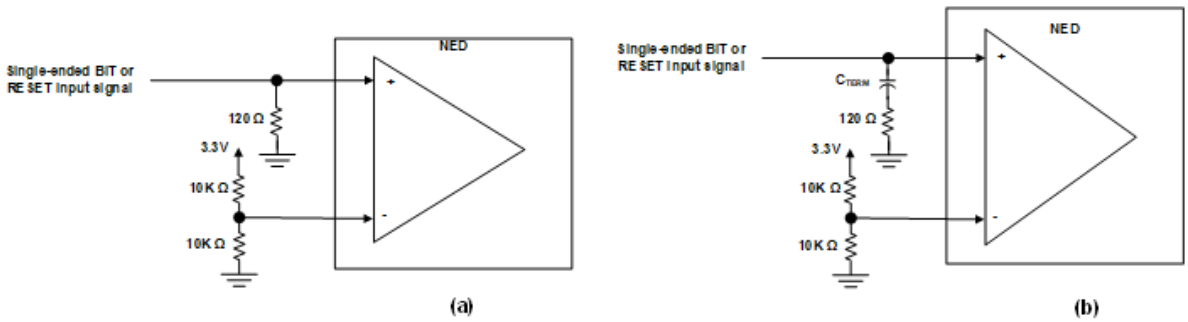

Figure 5. Single-Ended Input Signal Termination
(a) Simple Termination; (b) AC-Coupled Termination

As shown in Figure 5, the NED's BIT and RESET input signals can be operated as single-ended inputs. This requires that a reference voltage of approximately $V_{CC}/2$ = 1.65V be applied to the NED's BIT-L or NED_RST_L INPUT signal. In order to minimize power consumption for the driving circuit, similar to the circuit for differential input signals, it's recommended to include a series capacitor in series with the termination resistor, as shown in Figure 5(b). To minimize reflections, it's recommended that the RC time constant of the series RC termination be approximately equal to or greater than the anticipated pulse width.

4.2 Output Signals

The NED includes two pairs of differential output signals: NED_DET_H and NED_DET_H, which provide a differential pulse output that asserts following detection of a nuclear event; and NED_FLG_H and NED_FLG_L, which provide a latched flag differential output that also asserts following detection of a nuclear event. For the case of NED_FLG_H and NED_FLG_L, the latched flag output is de-asserted following reception of a minimum 250 ns pulse to the NED_RST_H and NED_RST_L differential RESET input.

Like the NED's input signals, its differential outputs may also be operated as single-ended signals.

4.2.1 Differential Outputs

For operating the NED DETECT and NED FLAG outputs as differential pairs, the signal pairs should be remotely terminated with 120 ohm resistors as shown in Figure 6. To reduce power consumption and dissipation by the NED's differential drivers, it's recommended to include a capacitor (C_{TERM}) in series with the termination resistor, as shown in Figure 6(b). This prevents the need for the NED drivers to supply current except during signal transitions between their high and low output states. To minimize reflections, it's recommended that the RC time constant of the series RC termination be approximately equal to or greater than the anticipated pulse width.

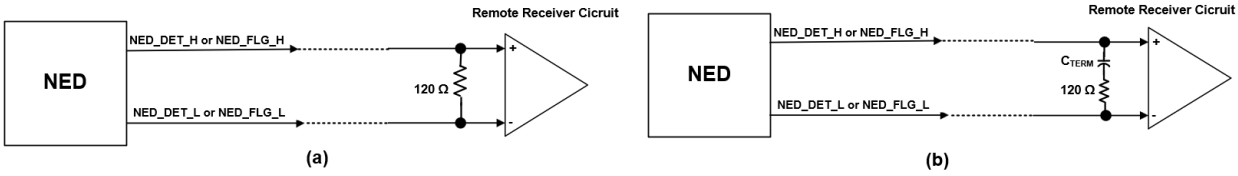

Figure 6. Differential Output Remote Signal Terminations
(a) Simple Termination; (b) AC-Coupled Termination

4.2.2 Differential Outputs

As shown in Figure 7, the NED's NED DETECT and NED FLAG output signals can be operated as single-ended outputs. This calls for a 120ohm termination between the signal and ground at the remote receiver circuit. In order to minimize power consumption for the NED driver, similar to the circuit for differential output signals, it's recommended to includes a series capacitor in series with the termination resistor, as shown in Figure 7(b).

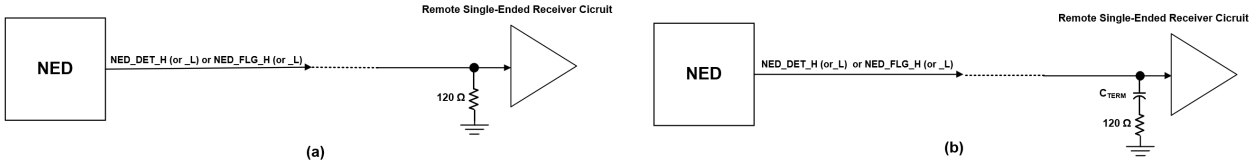

Figure 7. Single-Ended Output Remote Termination
(a) Simple Termination; (b) AC-Coupled Termination

4.3 Power Supply Crowbarring

One of the primary functions of the NED is to protect non-radiation hardened electronics from the effects of prompt dose radiation following a nuclear event. As shown in Figure 6, this involves using the NED output signal to activate a crowbar circuit to remove power from non-hardened circuits.

In Figure 8, the NED and crowbar circuit are powered by a hardened power supply. This is necessary to ensure that power for the NED itself and the crowbar circuit are able to operate through a nuclear event and the ensuing circumvention period by maintaining its output voltage.

Either the NED's pulse output (NED_DET_H/L) or latched flag output (NED_FLG_H/L) may be used for activating the power supply crowbar circuit. The pulse output provides a fixed duration time period to remove power from non-hardened loads, while the latched flag output requires a hardened processor, FPGA other circuit to deactivate the crowbar and restore power to non-hardened loads.

The crowbar circuits themselves must be built using radiation hardened components. In the example shown in Figure 8, the crowbar circuit operates by simultaneously disconnecting the power supply and providing a rapid discharge path to ground for decoupling capacitors for power voltages for non-hardened load circuits. The resistor in series with the MOSFET connecting to ground limits the current when discharging large capacitors on the power supply output.

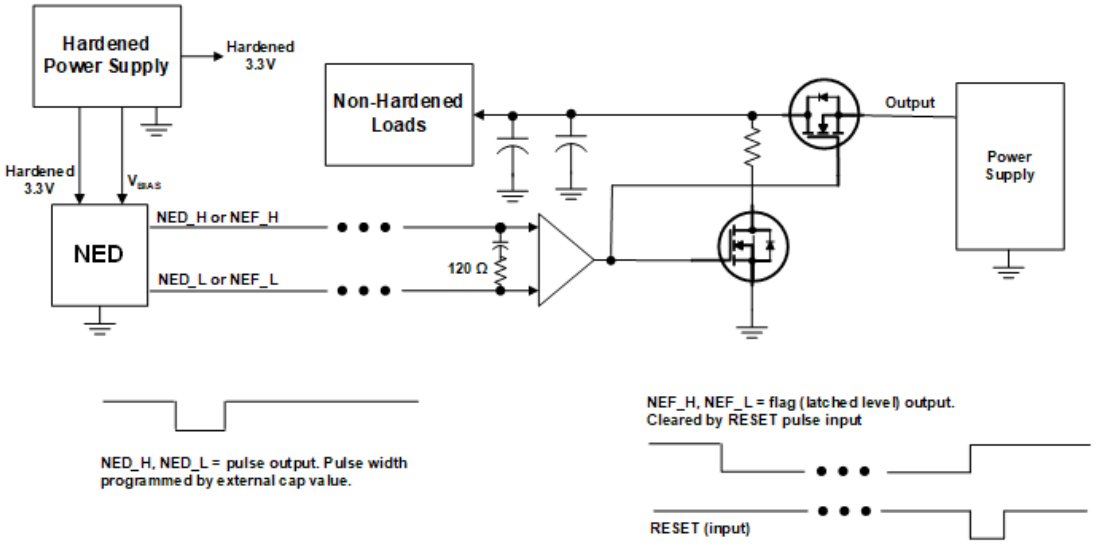

Figure 8. Using NED Output to Activate Power Supply Crowbarring

4.4 Shutting Down Processing

In addition to removing power from non-hardened electronics, another function of NEDs is to shut down digital processing following the detection of an event. As shown in Figure 9, this is done by connecting the NED's pulse or latched flag output to the input of a remote digital subsystem. As shown in this example, following the NED's detection of a nuclear event, the processing by a CPU or FPGA processor will be temporarily halted. In addition, this circuit includes a provision to prevent writing corrupt data to RAM or MRAM memory during the circumvention period.

If the NED_H and NED_L (pulse output) signals are used, the circumvention period is defined by the width of the NED_H/ NED_L pulse. This period is user-programmable by the selection of the PULSE WIDTH CAP (Figure 1) connected between the NED's pin 14 and ground. If the NEF_H and NEF_L (NED latched flag outputs) are used, then it will be necessary to assert the NED RESET signal at the end of the circumvention period. The circumvention period timing logic shown in Figure 9 will need to be hardened in order to operate reliably through the shut-down period for the processor and memory write logic.

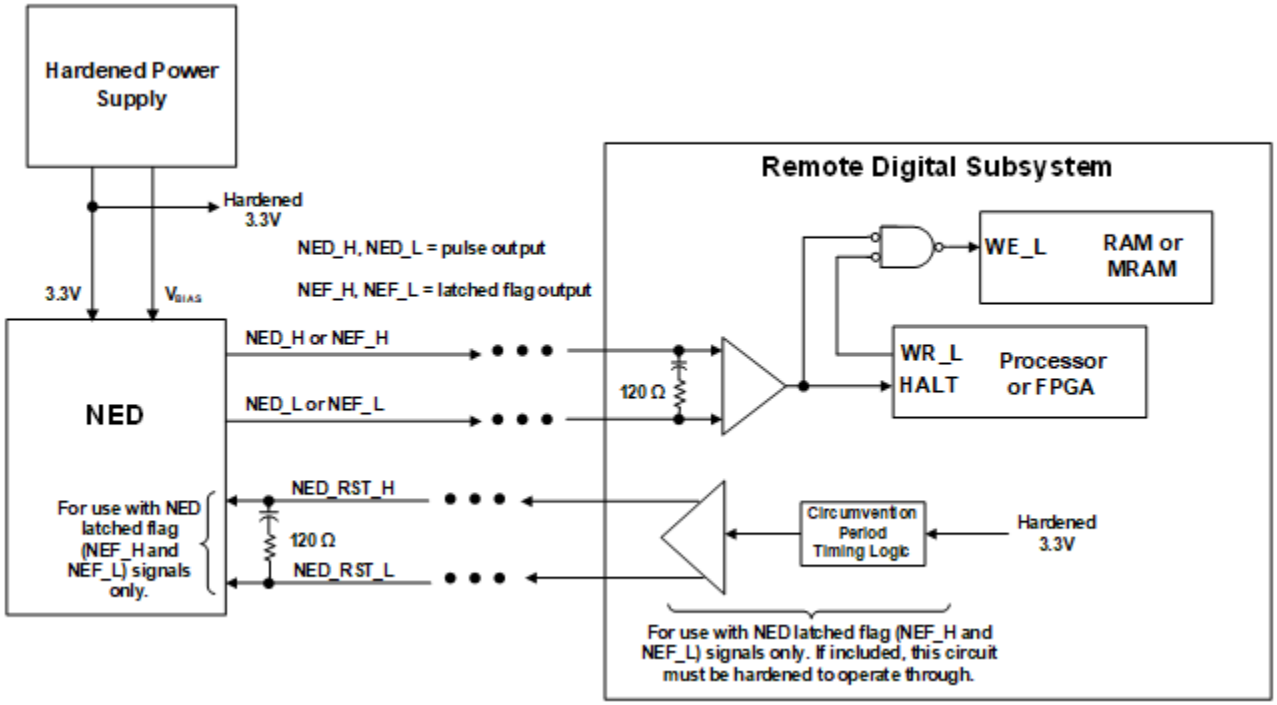

Figure 9. NED Output Shuts Down CPU and Memory Write Operations

5.0 Packaging

For the MYXRHNEDSCJ/X, the package size is a 17.53 x 17.53 x 3.05 mm (0.690 x 0.690 x 0.12 in.), 44-pin J-lead surface mount package. Figure 10 is the package outline drawing, while Figure 11 is the recommended PC board pad placement diagram.

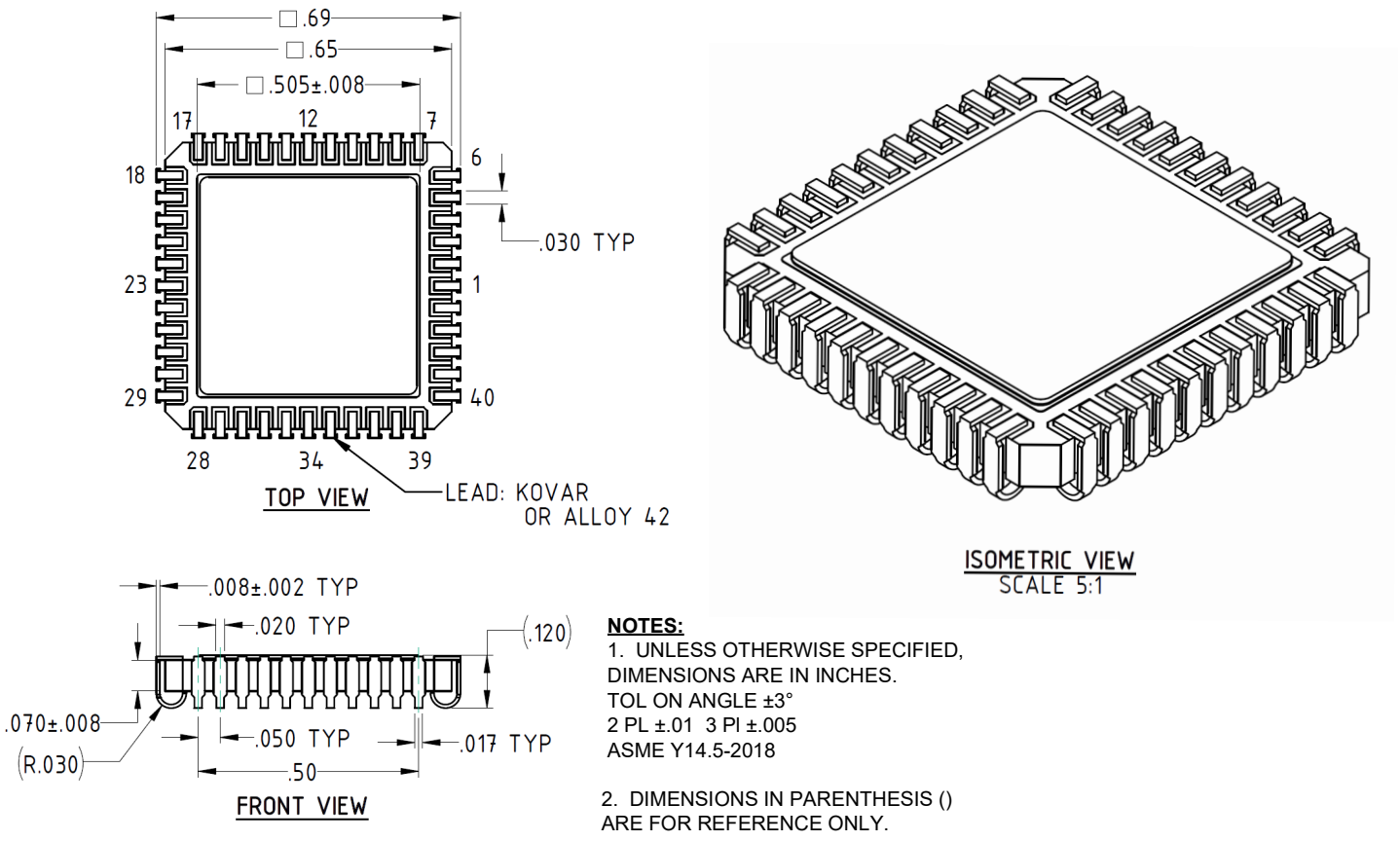

Figure 10. 44-pin J-Lead Surface Mount Package Outline

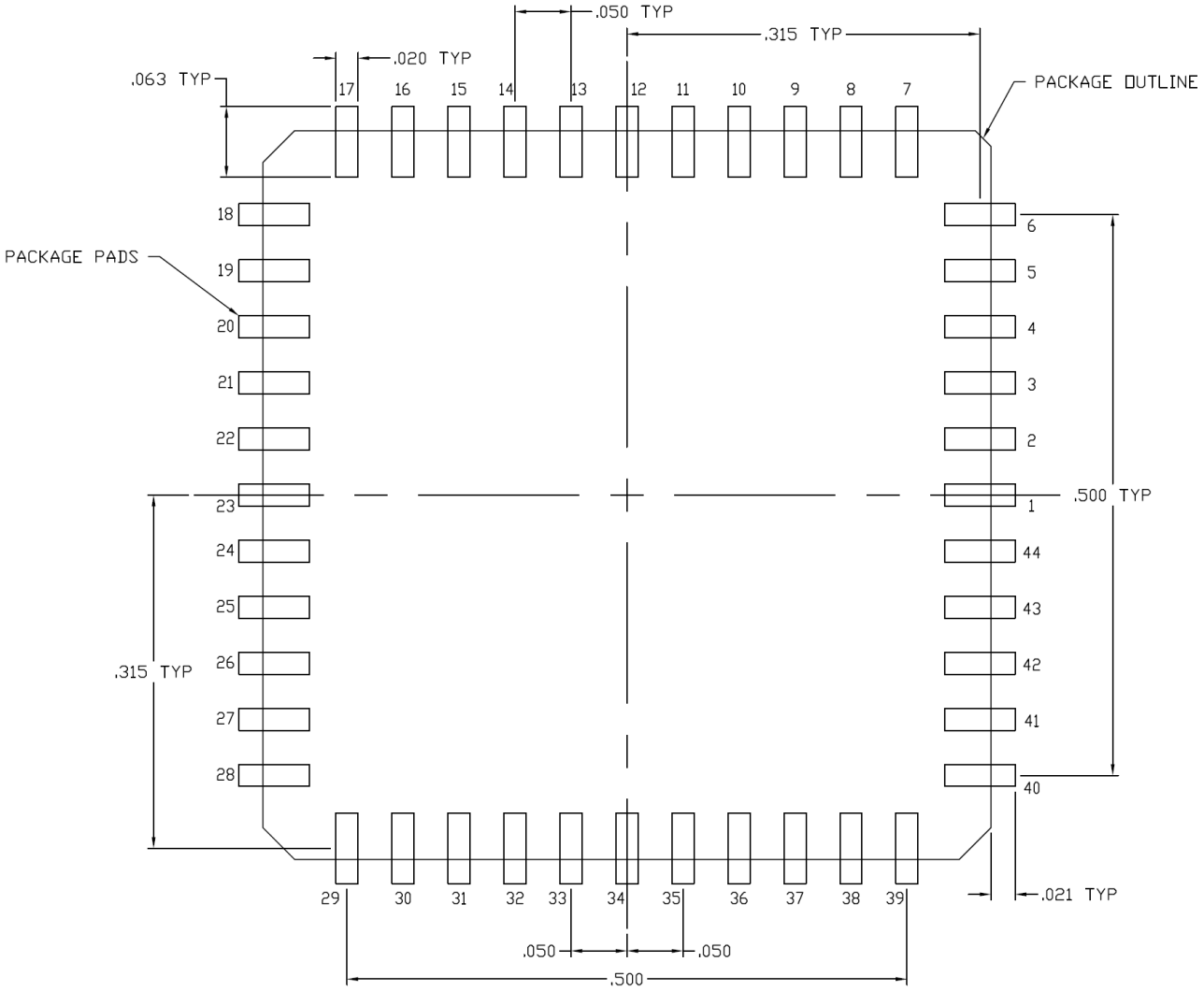

Figure 11. Recommended PC Board Pad Placement Diagram

6.0 Ordering Information

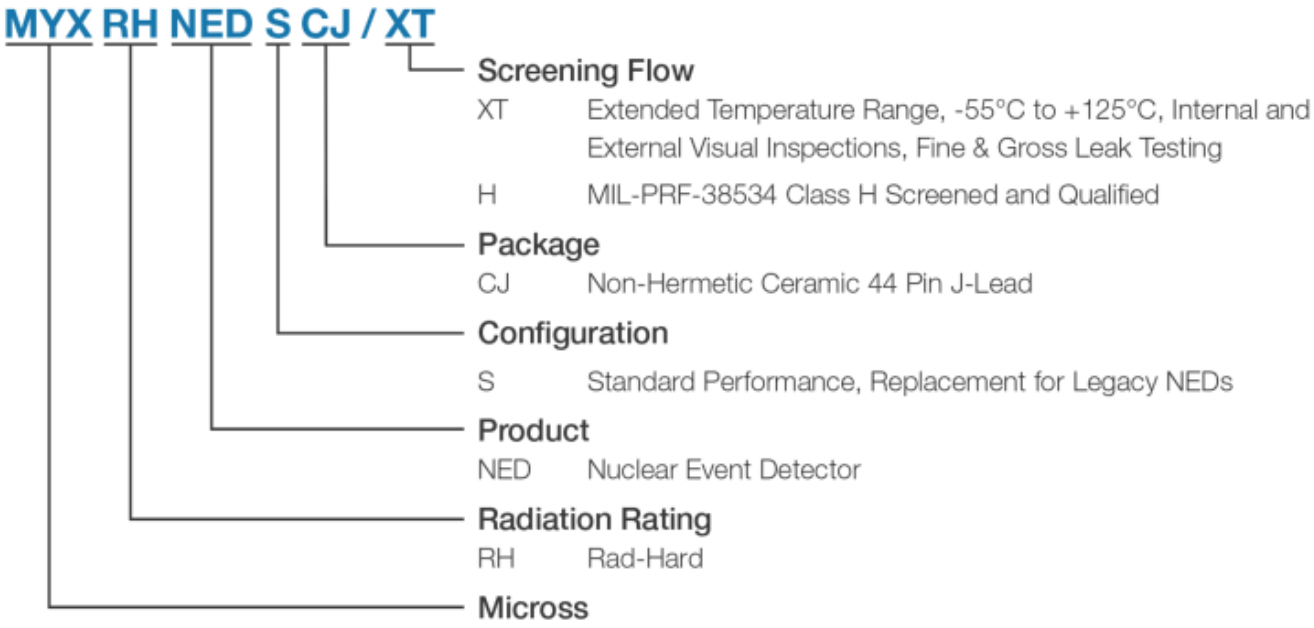

Table 4. Part Numbers

Part Number	Description
MYXRHNEDSCJ/XT	Extended temperature (-55 to +125 °C), Standard Performance, Hermetic, tested over -55 to 125 °C and leak tested; not qualified.
MYXRHNEDHCJ/H	Extended temperature (-55 to +125 °C), High Performance, Hermetic, MIL-PRF-38534 Class H qualified