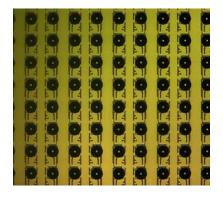
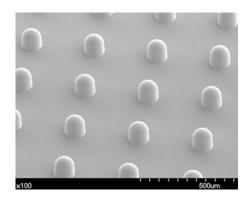
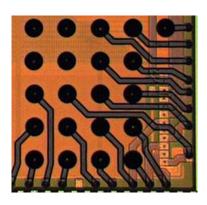


Wafer Level Packaging

Micross Advanced Interconnect Technology (Micross AIT) is home to one of the premier wafer bumping and wafer level packaging facilities in the U.S., with 20+ years of experience in developing and providing leading edge interconnect and integration technologies to customers around the world. We have the unique ability to support early stage development needs as well as low-to-mid volume production for more mature applications. Our ITAR-Registered facility supports wafer sizes up to 200mm with established and proven WLP processes and the flexibility to tailor unique solutions for your most demanding interconnect requirements.



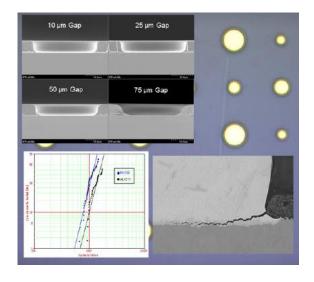




SOLDER BUMPING AND WAFER LEVEL CHIP SCALE PACKAGING

Micross AIT provides full in-house state-of-the-art wafer bumping and WLCSP solutions. Whether you have a need to process a single wafer or are looking for a source to provide recurring production services, Micross AIT has a wide array of WLP technologies.

- WLCSP ball place, electroplated C4, and Cu pillar bumping with bump diameters as small as 25 microns
- Bump-on-pad and bump-on-polymer processes
- Single and multiple layer Cu redistribution with several polymer repassivation material choices
- Eutectic Sn/Pb, Pb-free and high-Pb solder alloys
- Design services and custom test vehicle fabrication



ELECTRONIC MATERIAL CHARACTERIZATION AND PROCESS DEVELOPMENT

Micross AIT's extensive experience in flip chip and waferlevel packaging makes us an ideal partner for suppliers developing new materials for advanced packaging, such as photoresists, polymer dielectrics, plating chemistries and underfills.

- Process characterization and optimization
- Implementation into full process flows
- Test vehicle fabrication and reliability testing

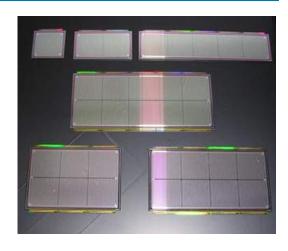


Wafer Level Packaging

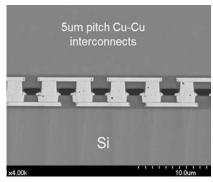
FLIP CHIP AND MULTI-CHIP MODULE ASSEMBLY

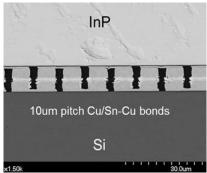
Micross offers a wide array of flip chip assembly capabilities, from single chip placements to multi-chip module and system-in-package assembly of multiple die and components.

- Flip chip assembly for single and multi-chip applications
- Precision die placement with accuracies better than +/- 0.5 microns
- Heterogeneous integration with Si, III-V and other device types
- Plasma Assisted Dry Soldering (PADS) Process enables true fluxless for assembly for Sn-bearing solders



METAL-METAL BONDING FOR 2.5/3D TECHNOLOGIES





2.5D and 3D integration technologies are driving the integration of devices with extremely high interconnect densities for Si interposer and chip stacking applications.

- Solid/liquid interdiffusion assembly with CuSn-Cu bump arrays demonstrated down to 10 micron pitch
- Cu/Cu thermocompression bump bonding demonstrated down to 5 micron pitch
- Solutions for chip stacking and high thermal stability interconnects that remain solid at high temperatures

More Information: Alan Huffman, Director of Engineering 919.248.9216

Micross Advanced Interconnect Technology 3021 E. Cornwallis Road, PO Box 110283 Research Triangle Park, NC 27709

About Micross

Micross (www.micross.com) is the global one-source provider of Bare Die & Wafers, Advanced Interconnect Technology, Custom Packaging & Assembly, Component Modification Services, Electrical & Environmental Testing and Hi-Rel Products to manufacturers and users of semiconductor devices. In business for more than 40 years, our extensive hi-reliability capabilities serve the Aerospace & Defense, Space, Medical and Industrial markets. Micross possesses the sourcing, packaging, assembly, engineering, test and logistics expertise needed to support an application throughout its entire program cycle.