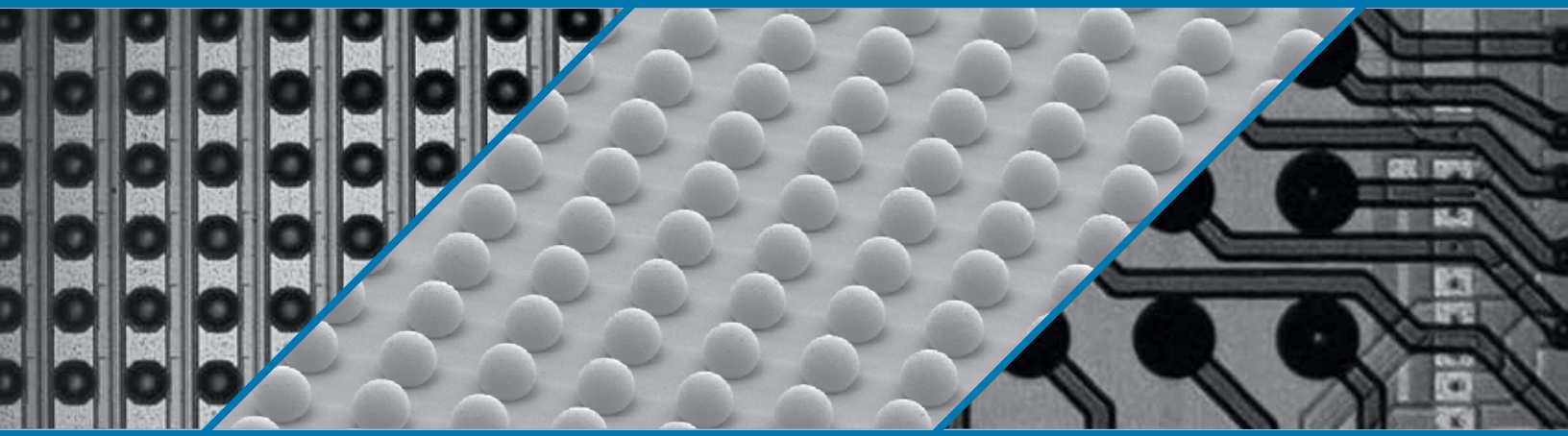
micross®
one source. one solution.®

Wafer Level Packaging

Service Overview



Micross Advanced Interconnect Technology (AIT) is home to one of the premier wafer bumping and wafer level packaging facilities in the US. With over 25+ years of experience in developing and providing leading edge interconnect and integration technologies to customers around the world.

SOLDER BUMPING AND WAFER LEVEL CHIP SCALE PACKAGING

Micross has the unique ability to support early stage development needs as well as low-to-mid volume production for more mature applications. Our ITAR-Registered facility supports wafer sizes up to 200mm with established and proven WLP processes and the flexibility to tailor unique solutions for your most demanding interconnect requirements.

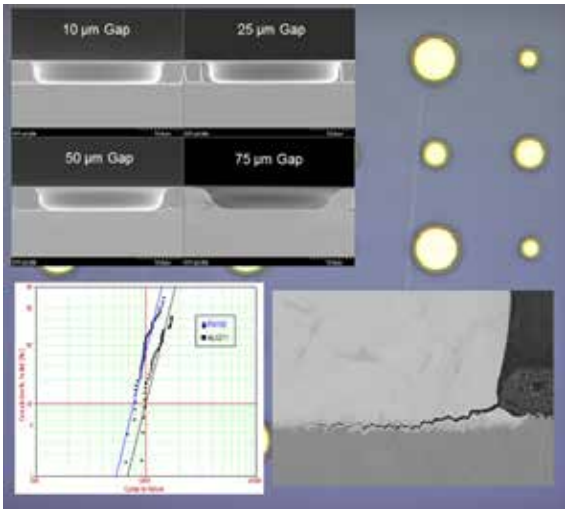
Micross provides full in-house state-of-the-art wafer bumping and WLCSP solutions. Whether you have a need to process a single wafer or are looking for a source to provide recurring production services, Micross has a wide array of WLP technologies.

- WLCSP Ball Place, Electroplated C4 and Cu Pillar Bumping with Bump Diameters as Small as 25µm
- Bump-On-Pad and Bump-On-Polymer Processes
- Single and Multiple Layer Cu Redistribution with Several Polymer Repassivation Material Choices
- Eutectic Sn/Pb, Pb-Free and High-Pb Solder Alloys
- Design Services and Custom Test Vehicle Fabrication

ELECTRONIC MATERIAL CHARACTERIZATION AND PROCESS DEVELOPMENT

Micross extensive experience in flip chip and wafer-level packaging makes us an ideal partner for suppliers developing new materials for advanced packaging, such as photoresists, polymer dielectrics, plating chemistries and underfills.

- Process Characterization and Optimization
- Implementation into Full Process Flows
- Test Vehicle Fabrication and Reliability Testing

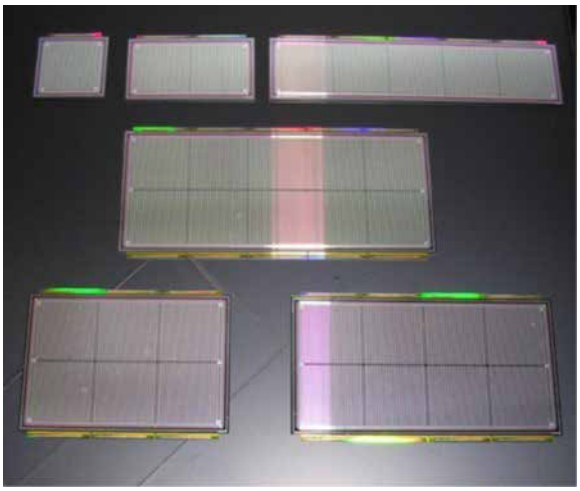


Wafer Level Packaging

FLIP CHIP & MULTI-CHIP MODULE ASSEMBLY

Micross offers a wide array of flip chip assembly capabilities, from single chip placements to multi-chip module and system-in-package assembly of multiple die and components.

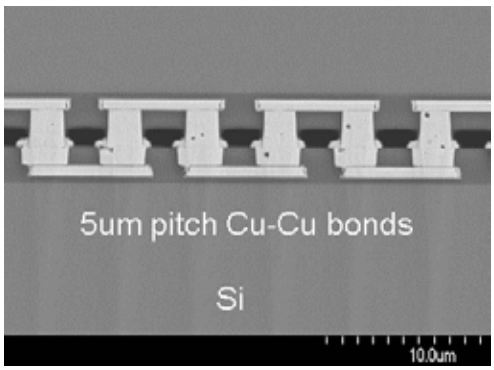
- Flip Chip Assembly for Single and Multi-Chip Applications
- Precision Die Placement with Accuracies Better than +/- 0.5µm
- Heterogeneous Integration with Si, III-V and Other Device Types
- Plasma Assisted Dry Soldering (PADS) Process Enables True Fluxes for Assembly for Sn-Bearing Solders

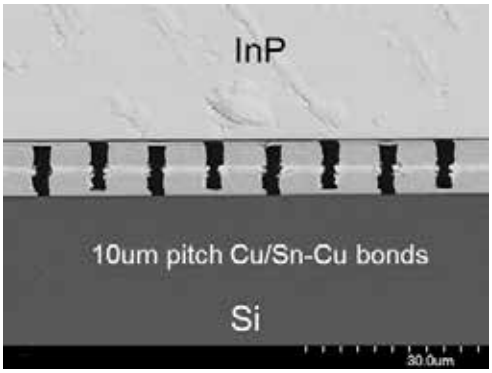


METAL-METAL BONDING FOR 2.5/3D TECH.

2.5D and 3D integration technologies are driving the integration of devices with extremely high interconnect densities for Si interposer and chip stacking applications.

- Solid/Liquid Inter-Diffusion Assembly with CuSn-Cu Bump Arrays Demonstrated Down to 10µm Pitch
- Cu/Cu Thermo-Compression Bump Bonding Demonstrated Down to 5µm Pitch
- Solutions for Chip Stacking and High Thermal Stability Interconnects that Remain Solid at High Temperature





About Micross

Micross is the most complete provider of advanced microelectronic services and component, die and wafer solutions. With the broadest authorized access to die & wafer suppliers, an extensive portfolio of hi-rel power, RF, optoelectronics, memory, data bus, logic, and SMD/5962 qualified products, and the most comprehensive advanced packaging, assembly, modification, upscreening, and test capabilities, Micross is uniquely positioned to provide unparalleled high-reliability solutions, from bare die, to fully packaged devices including hermetic ICs/MCMs, PEMs, ASICs, FPGAs, and PCBs, to complete program life-cycle sustainment. For more than 45 years, Micross has been a trusted source for the aerospace, defense, space, medical, energy, communications, and industrial markets.

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