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Process Qualification Summary

For

KA113 GaAs Amplifier

Revision 2: 06/16/2020

Prepared by

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Contents

1.0 SUMMARY 3

2.0 APPLICABLE DOCUMENTS 3

3.0 FOUNDRY PROCESS QUALIFICATION INFORMATION 3

4.0 PRODUCT QUALIFICATION TESTING 4

1.0 SUMMARY

This report is a summary of qualification results associated with the KA113 GaAs Low Noise Amplifier. It includes foundry process data as well as product qualification data.

2.0 APPLICABLE DOCUMENTS

MIL-PRF-38535	General Specification for Integrated Circuits Manufacturing
MIL-STD-883	Test Method Standard, Microcircuits
JS-001-2014	Electrostatic Discharge Testing, Human Body Model
JS-002-2014	Electrostatic Discharge Testing, Charge Device Model

3.0 FOUNDRY PROCESS QUALIFICATION INFORMATION

This device is manufactured on a 0.25µm pHEMT E-mode T-gate process that is well suited for high frequency, low noise applications. Representative transistors from this process were subjected to the following test regime:

1. PCM verification
2. HTOL (High Temperature Operating Life Test)
3. Biased HAST (Biased Highly Accelerated Stress Test)
4. TCT (Temperature Cycling Test)
5. TH (Temperature Humidity Test)
6. THB (Temperature Humidity Bias Test)
7. ESD (Electrostatic Discharge Test)
8. MIM Cap Voltage Ramp Test

According to the HTOL test results of the E-mode active transistor devices, the predicted MTTF at a junction temperature (Tj) of 125C is 28.3 million hours under an assumed activation energy of 1.1eV. PCM units passed all of the above requirements as defined by the device manufacturer. Due to the proprietary nature of the device manufacturer, KCB has possession of the foundry test report, however, however, the report cannot be directly published. Please contact KCB for additional details with respect to foundry process qualification testing.

4.0 PRODUCT QUALIFICATION TESTING

4.1 ESD TESTING

Devices were tested IAW JEDEC JS-001-2014 (HBM) and JS-002-2014 (CDM). The results of the testing indicate that the device is Class 1B.

4.2 TEMPERATURE CYCLING

Three lots of 77 devices were subjected to temperature cycling IAW JESD22-A104 for 500 cycles -65C to +150C. All devices passed testing subsequent to being exposed to this regime.

4.3 HIGH TEMPERATURE STORAGE LIFE

Three lots of 77 devices were subjected to high temperature storage life IAW JESD22-A103 for 1000 hours at TA = +150C. All devices passed testing subsequent to being exposed to this regime.

4.4 LOW TEMPERATURE STORAGE LIFE

Three groups of 5 devices were subjected to low temperature storage life IAW MIL-STD-810G, Method 502.5, 2 hours at TA = -65C. All devices passed testing subsequent to being exposed to this regime.

4.5 OPERATING LIFE

Twenty-five devices chosen at random from two wafer lots were subjected to operating life IAW MIL-STD-883, Method 1005 for 2000 hours at T_J = +170C. All devices passed testing after being exposed to this regime. Test data regarding this testing is available upon request.