Considerations in Converting from SMT to Die Assemblies

National Semiconductor Technical Seminar Series

Die Product Business Unit

Approaches, Options & Solutions

- Die conversion trends and drivers
- Die interconnect approaches
- Device and information resources
- Implementation

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Die Conversion Trends & Drivers

- Form factor
- Integration
- Performance
- Reliability

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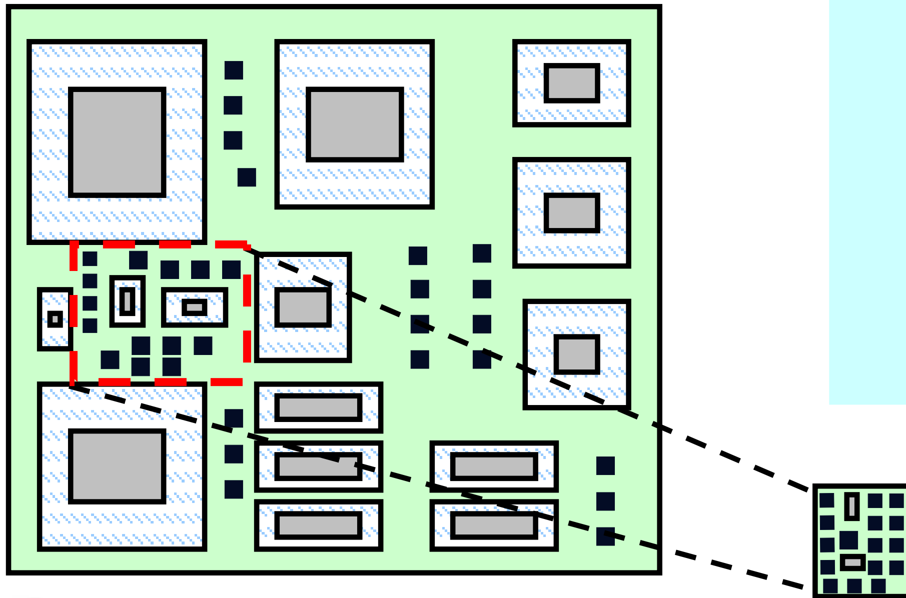
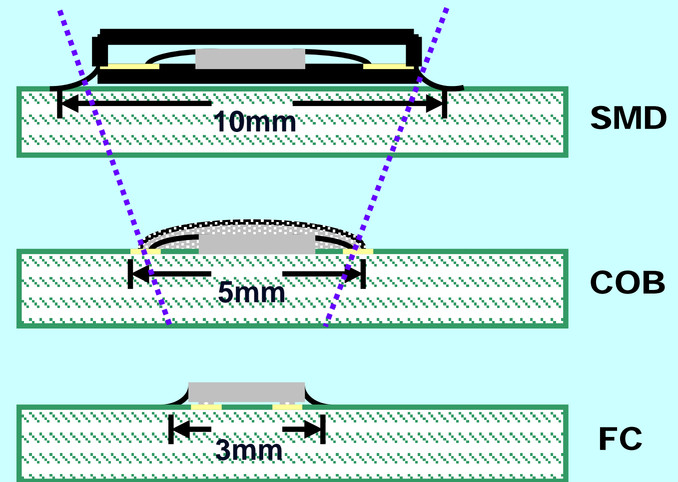
Form Factor / Integration

Improved Integration



“Daughter board”

Reduced Size



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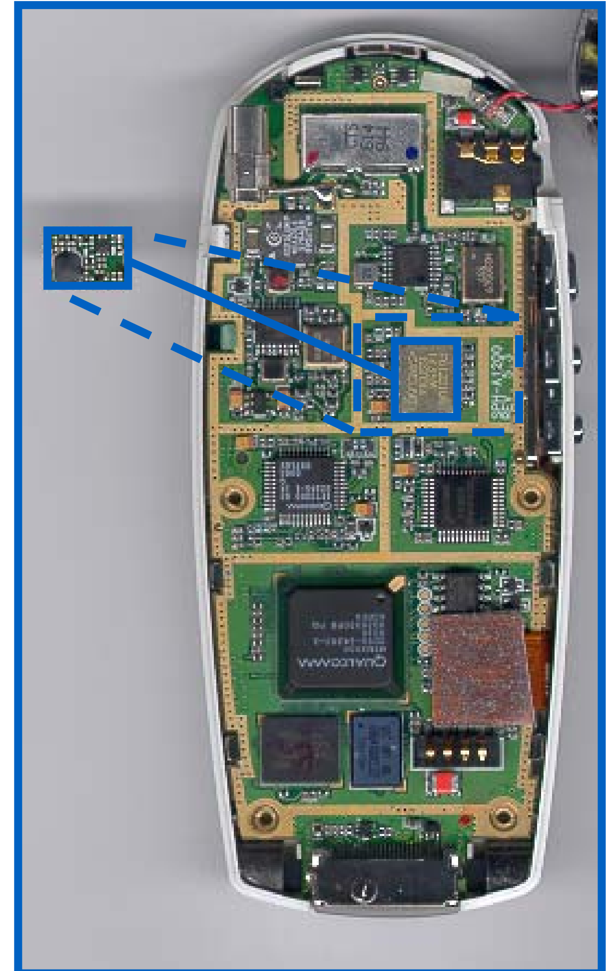
Form Factor / Integration

- **Impact on current model**
  - **≈ 25% of size**
  - **≈ 50% weight**
  - **Same height**
  - **Improved testability**
  - **Increased reliability**



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Form Factor / Integration

Height variations of packaging approachs

Total package height (mils)

160
140
120
100
80
60
40
20
0

PLCC
DIP
SOIC
QFP
SSOP
TQFP
CSP
TSSOP
LLP
COB
Flip Chip

Minimum Effective Height

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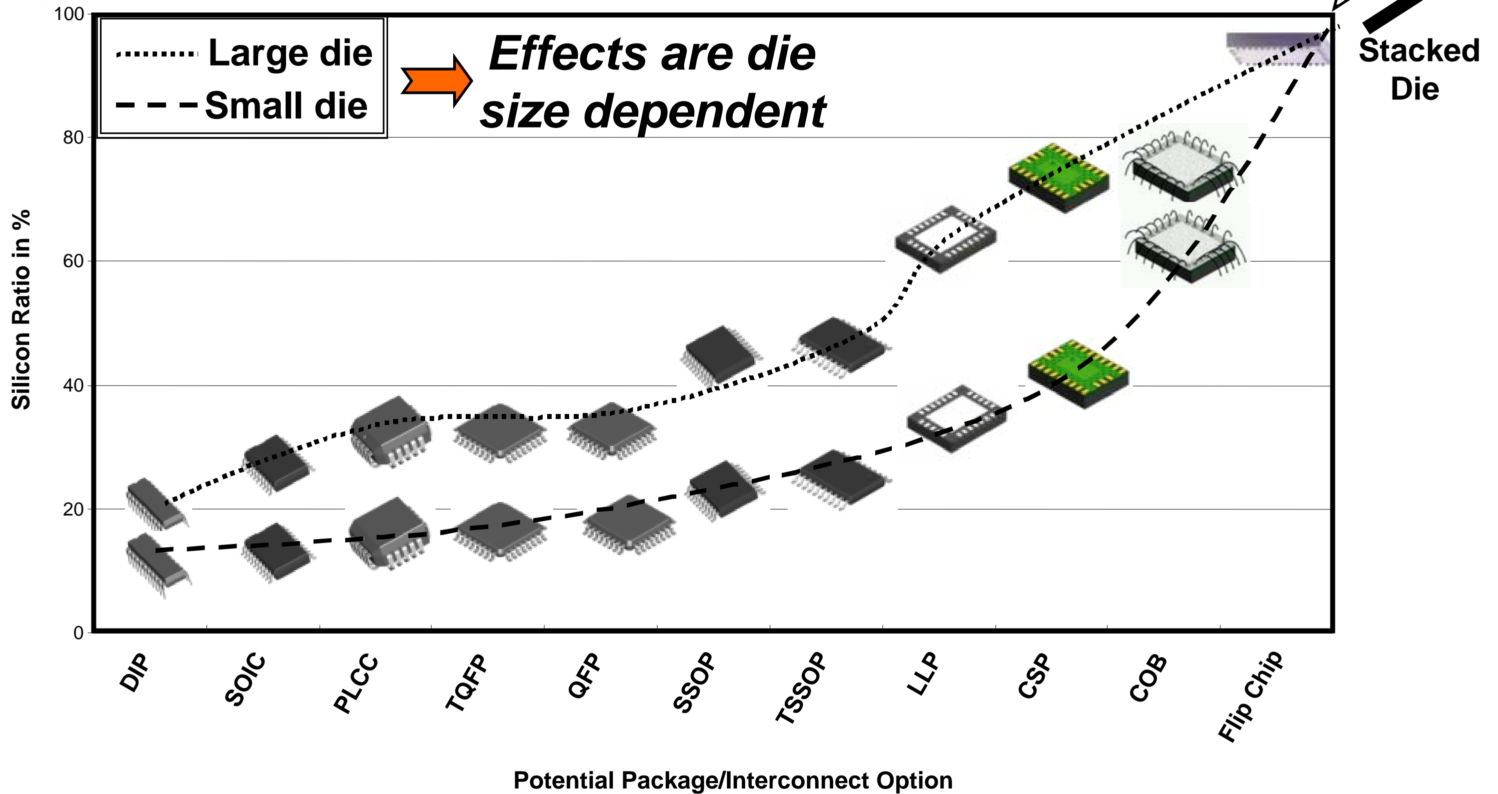
Form Factor / Integration



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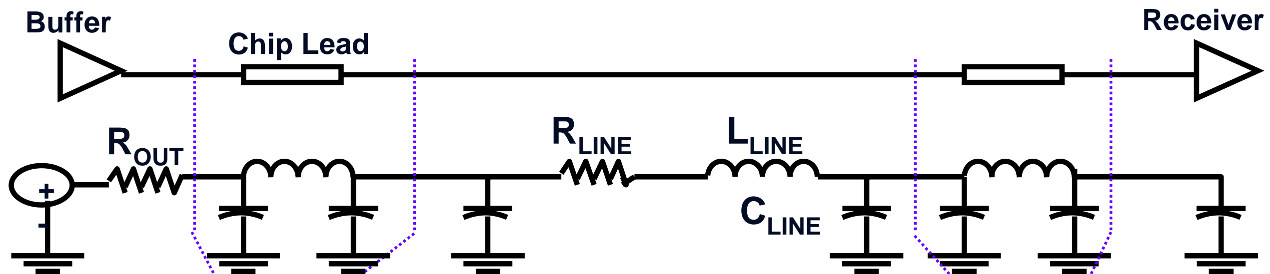
Performance

- Improved Electrical Performance
  - Shorter Interconnections
    - Inductance / capacitance
    - Power / ground distribution



Lead Type	pF	nH
SMD	1	1 - 12
PGA	1	2 - 5
Wire Bond	0.5	1 - 3
Solder Bump	0.1	0.01

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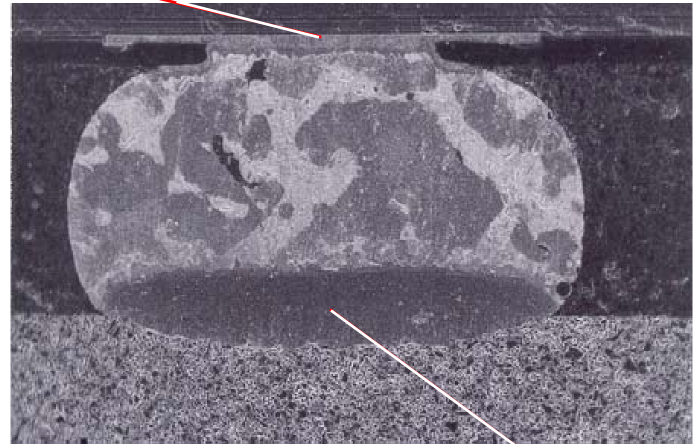
Reliability

- Improved die Reliability due to Reduced Connections



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Die Interconnect Approaches

- Wire Bond
  - Aluminum wedge
  - Gold ball
- Flip Chip
  - Solder
  - Anisotropic adhesive
  - Gold
- Trade offs

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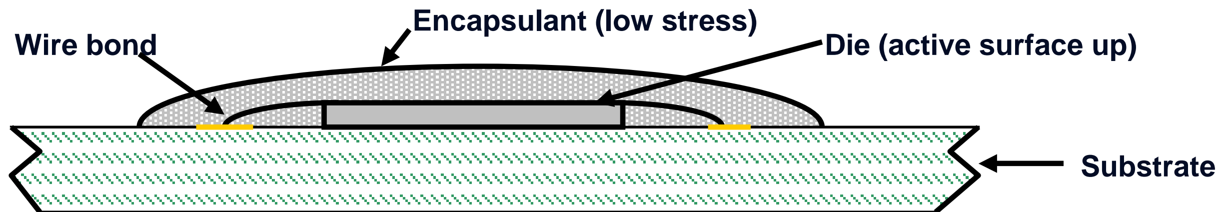
Wire Bond

- **Bare die utilizing wire bond technology**

COB: Chip-on-board (wire bond)



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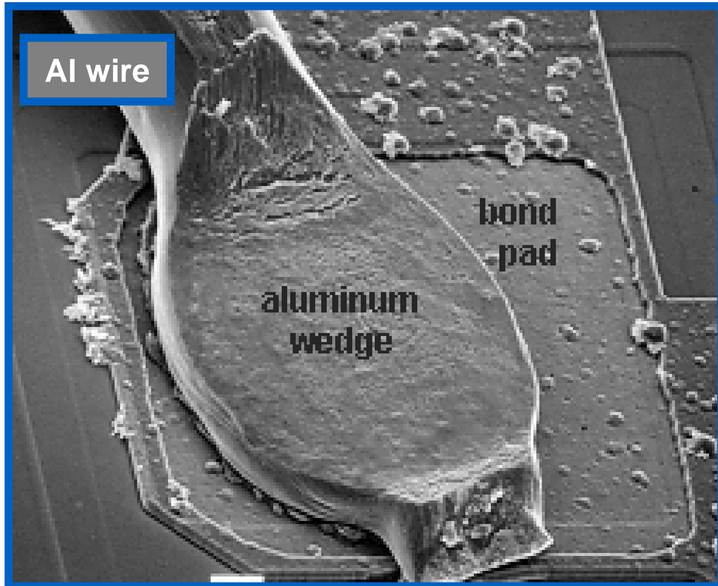
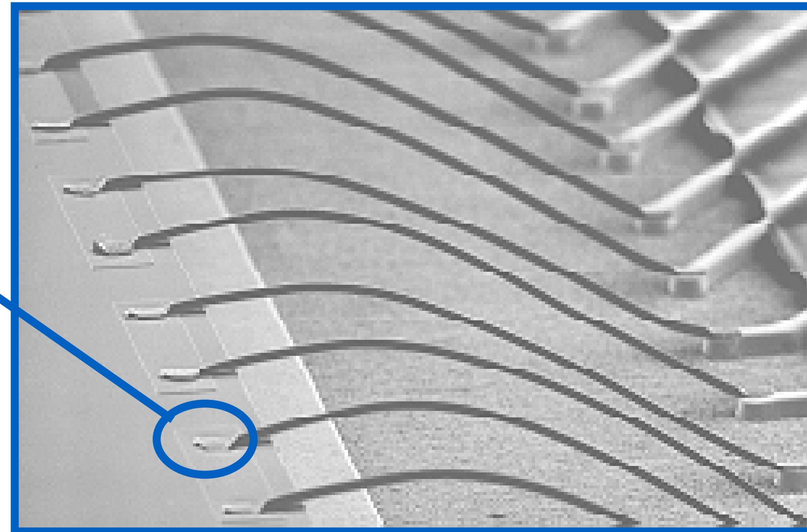
Wire Bond

- Common COB wire bond types
  - Al wedge bond





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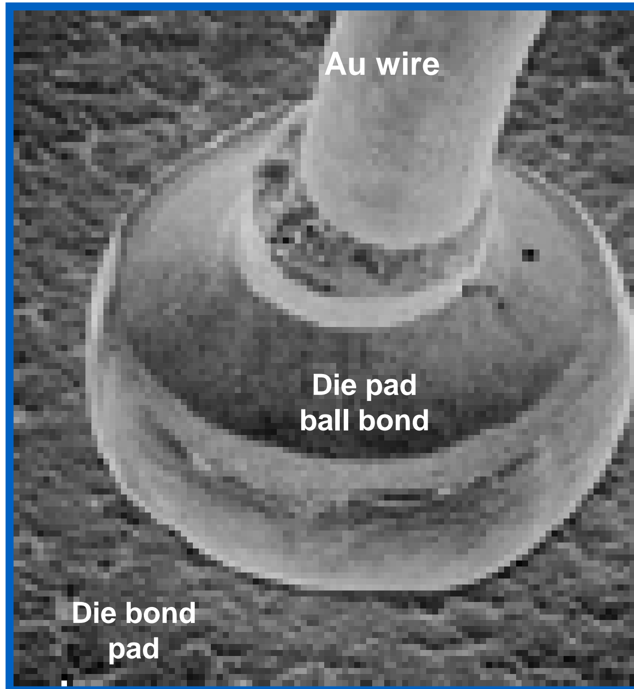
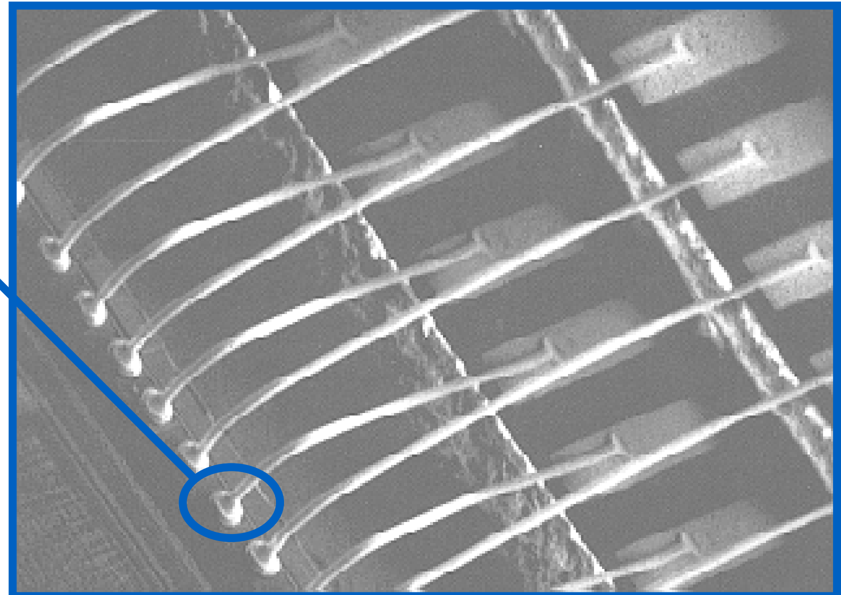
Wire Bond

- Common COB wire bond types
  - Au ball bond





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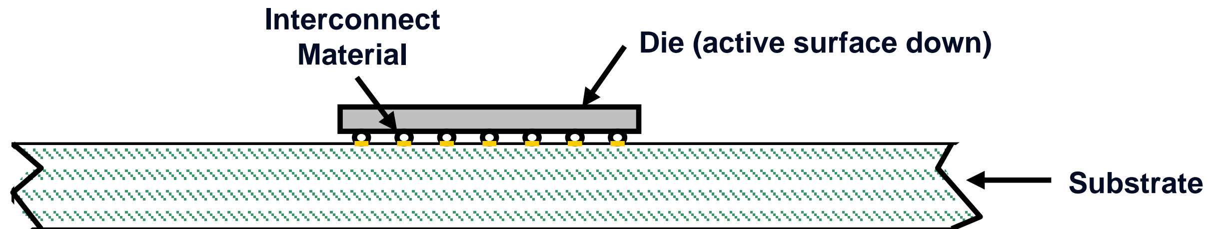
Flip Chip

- Bump layout
  - Peripheral
  - Area array



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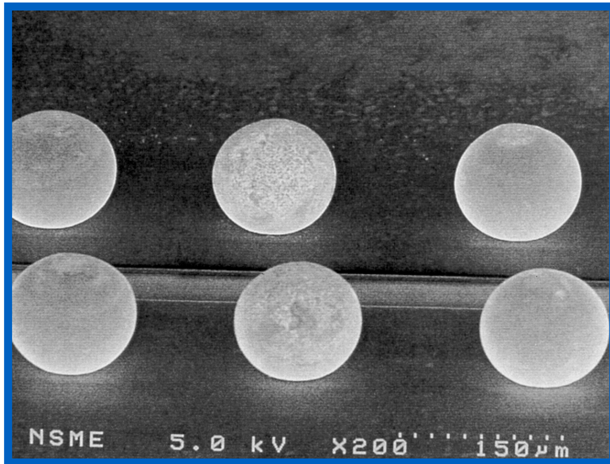
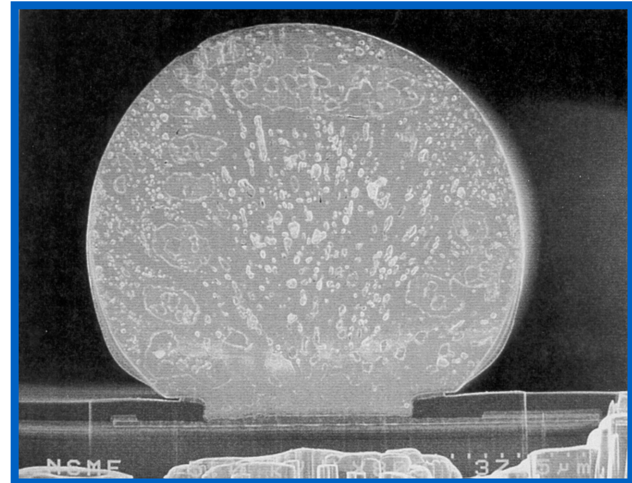
Flip Chip

- Solder Bump Flip Chip
  - High lead solder
  - Eutectic solder (63% Sn, 37% Pb)
  - Lead-free solders





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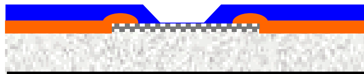
Flip Chip
- Solder Bump Build-up

Starting Bond Pad

Spin on BCB

Define Pad Opening



Sputter/Evaporate UBM

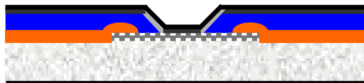
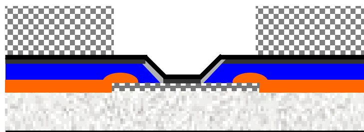
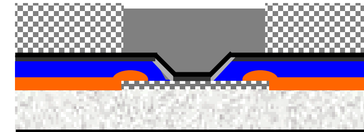
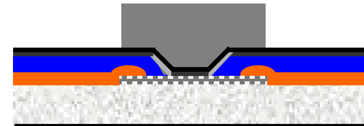


Image Solder Dam

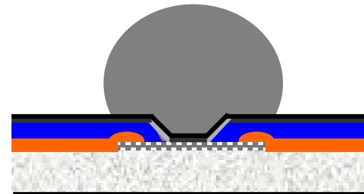




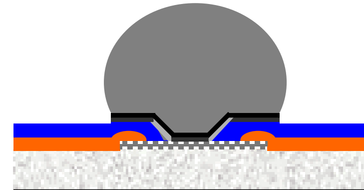
Electroplate Solder



Strip Dam Template



Reflow Solder



Etch UBM

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Flip Chip

- **Anisotropic Conductive Adhesive (ACA)**

Specialized applications:
LCD, display drivers

Temperature

Pressure

Die

Bumped Pad

ACF

Trace Pad

Substrate

Time

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Flip Chip

- Gold Flip Chip Attach

Ball Attach

Wire preparation

Specialized applications: LCD, medical, disk drives

Bond tool

Bond Pad

Initial Ball

Stud Formation

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Tradeoffs
I/O capability COB v flip chip

150um bumped array

I/O Pads / Die
Thousands

12
10
8
6
4
2
0

6 8 10 12 14 16

600 mils

Die Size (mm)

100um wire bond

WB - 100um
WB - 100um 3 rows
WB - 70um
WB - 70um 3 rows
Area array 225um
Area array 150um

Courtesy IBM Microelectronics

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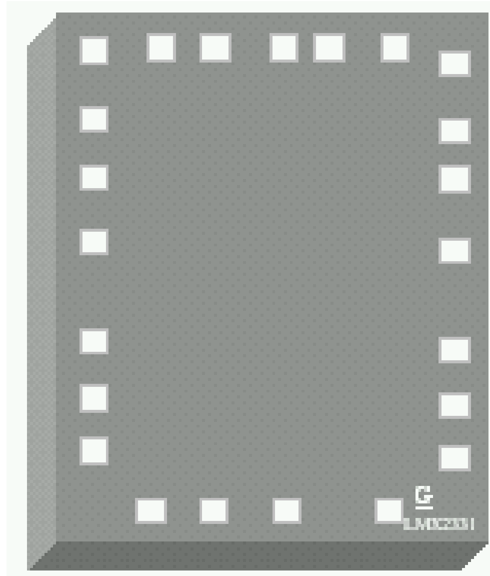
Tradeoffs

- **Peripheral Bond Pads - COB**



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Tradeoffs - COB

- **Advantages**
  - Reliable connection
  - Manufacturing experience
  - Low volume – cost effective
  - Die availability
- **Challenges**
  - Overmold / glob-top req’d
  - High pin counts
  - Bond pad pitch & pad size
  - High volume manufacturing
  - Arrays and staggered bond pads
  - Mixed with SMT

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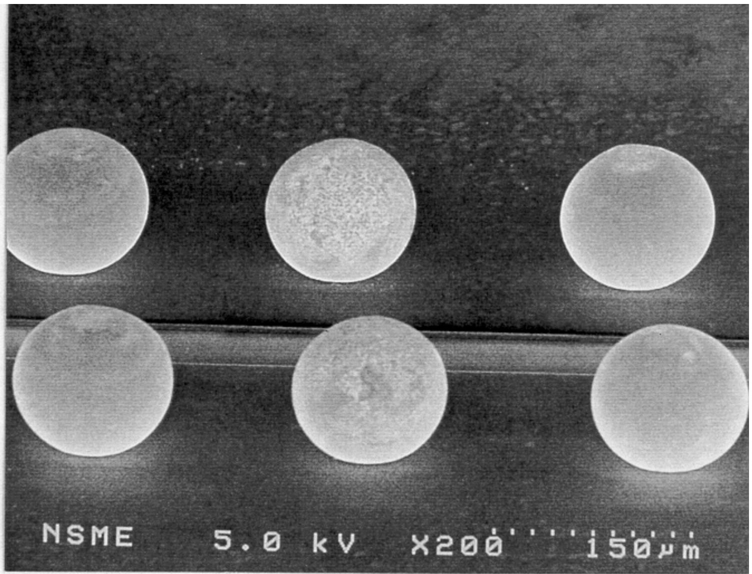
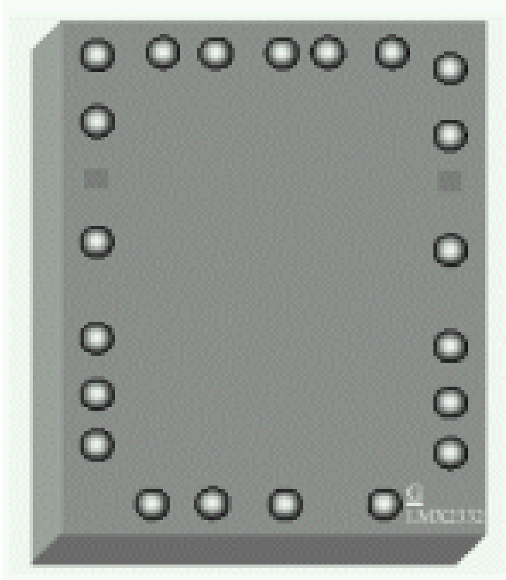
Tradeoffs

- Peripheral Array Solder Bumps
  - Pitch
  - Routing





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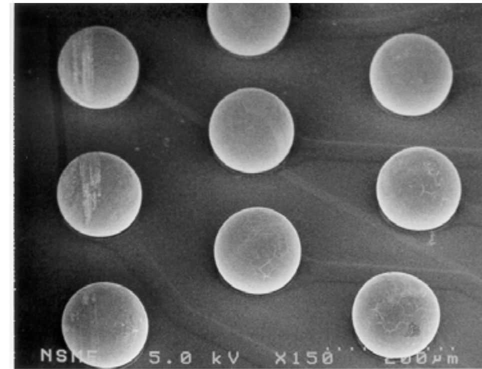
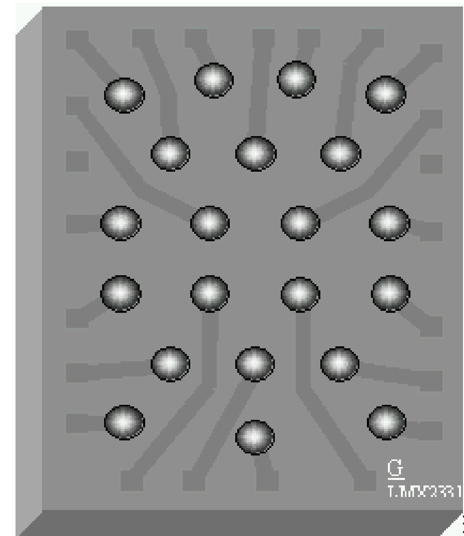
Tradeoffs

- Area Array Solder Bumps
  - Size
  - Design flexibility
  - Routing
  - Pitch





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Tradeoffs - Flip Chip

- **Advantages**
  - **Smallest footprint per active circuitry**
  - Increased functionality per substrate area
  - Improved thermal capability
  - Lower cost in volume processing
  - **Improved performance R, L, C**

- **Challenges**
  - Handling and die placement
  - Lack of standard bump technology
  - Cost effective high density substrates
  - **CTE matched or underfill - reliability**
  - **Product availability & need for redistribution**
  - Industry infrastructure

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Tradeoffs

Technology Comparison

	SMT	COB	Flip Chip
Size	Good	Better	Best
Component integration	Good	Better	Best
Process complexity	Best	Better	Good
I/O count	Good	Better	Best
Performance	Good	Better	Best
Manufacturability	Best	Best	Good
Cost	Better	Best	Best?

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Supplier & General Information Resources

- Multiple functions available
  - Die suppliers

- Information
  - Interconnect
  - Performance
  - Consortiums & Standards Organizations
  - Outsourcing

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Supplier & General Information Resources

- Interconnect
  - National Semiconductor: www.national.com
  - Kulicke & Soffa: www.kns.com
  - Unitive: www.unitive.com
  - G. Riley: www.flipchips.com
  - Georgia Tech: www.marc.gatech.edu
  - Trade shows and symposiums
    - HDI / PCB: www.hdiexpo.com, www.pcbwest.com
    - IMAPS: www.imaps.org
    - ECTC: www.ectc.net
    - SMT: www.smta.org
    - China International IC

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Supplier & General Information Resources

- Consortiums & Standards Organizations
  - Die Products Consortium: www.dieproduct.com
  - High density packaging user group: www.hdpug.org
  - Good Die: www.gooddie.net
  - Cenelec: www.cenelec.org

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Supplier & General Information Resources

- Outsourcing
  - Flextronics: www.flextronics.com
  - Solectron: www.solectron.com
  - Celestica: www.celestica.com
  - SCI / Sanmina: www.sanmina.com
  - Others world wide

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Supplier & General Information Resources

- Performance options
  - “Known Good Die”
    - Performance guarantee
    - Testing strategies
  - “Pretty Good Die”
- Quality
- Other… buyer beware!

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Implementation

- Converting from SMT to COB or flip chip

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Implementation

- **COB process flow**

Adhesive Application

Die Placement
&
Adhesive Cure

Wire Bond

Encapsulation

Paste Dispense and Die Attach

Cure Oven

Plasma Clean

Wire Bond

Glob Top Dispense

Cure Oven

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Implementation

- Equipment conversion strategies
  - COB
    - Adhesive dispense
    - Die attach
    - Plasma clean
    - Wire bond
    - Encapsulation

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Implementation

- **Flip chip process flow**

Solder bump

Flux dipping | Alignment | Placement | Reflow soldering | Flux cleaning | Under-fill dispense and cure

Flux dip and flip chip mount

Reflow Oven

Flux Clean

Under-fill Dispense

Cure Oven

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Implementation

- Equipment conversion strategies
  - Flip Chip
    - Flux application
    - Chip placement
    - Reflow
    - Underfill

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