

Starting Design

Alun D. Jones

Micross Components Ltd.



Contents

- The Tools
- The Technologies
- Design Libraries
- The Future and Obsolescence
- The Design Flow
- The Information Routes
- Project Costing

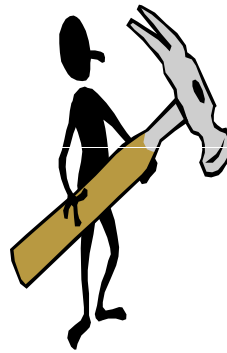
Design Tools

The Design Equipment
& the Designer



Tools of the Trade

- Schematic Capture & netlister
- VHDL entry system
- Analog simulator
- Digital simulator
- Mixed Signal simulator
- Design Synthesis
- Layout Floorplanner
- Manual Layout
- Automatic Layout
- DRC / ERC / LVS Tools
- Back Annotation Tools
- Failure / Fault Analysis Tools

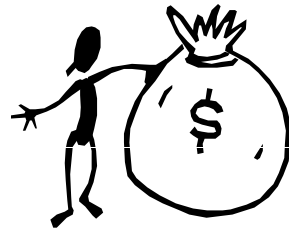


Artist, AutoCad
Text Editor
Spice 2G6, Spectre
Verilog, Silos
Spectre-Verilog-XL
Synopsis, Synergy
PreView
Physical Artist
Cell Ensemble
Dracula, Diva
Diva
VeriFault, VeriTime

- **A GOOD BACKUP & ARCHIVE SYSTEM**

Design Seat Costs

• Workstation & ancillaries SUN Sparc		£17,000
• Design / Capture	Analog Artist	£35,000
• Digital Simulator	Verilog	£22,000
• Analog Simulator	Spectre	£24,000
• Layout	Artist Layout	£45,000
• Floor Planner	PreView	£25,000
• VHDL synthesizer	Synopsis	£23,000
• Auto Place-Route	Cell 3	£70,000
• Fault Grader / Timing Anal.	VeriFault+	£22,000
• DRC/ERC/LVS/Extract	Dracula	£45,000
• Training		£10,000



• **TOTAL**

£BIG

The Designers Customers

- Contracting Customer
- Sales Engineer !
- Silicon Vendor (Fab House)
- Mask Manufacturer
- Packaging House
- Test House
- Quality Department
- Production

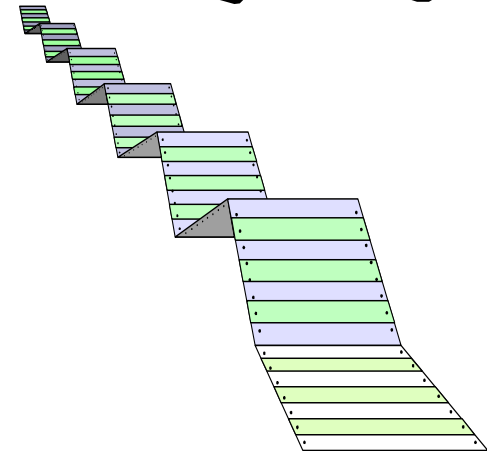
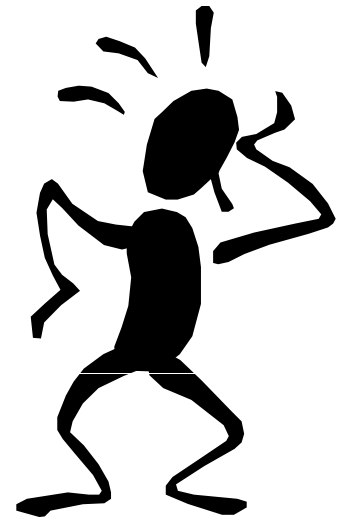


Responsibilities and Duties

- Realizable and practical ASIC design
- Clear and unambiguous data to ALL his customers
- Schematics, simulation & verification results
- Bonding and packaging information
- Test and operational data

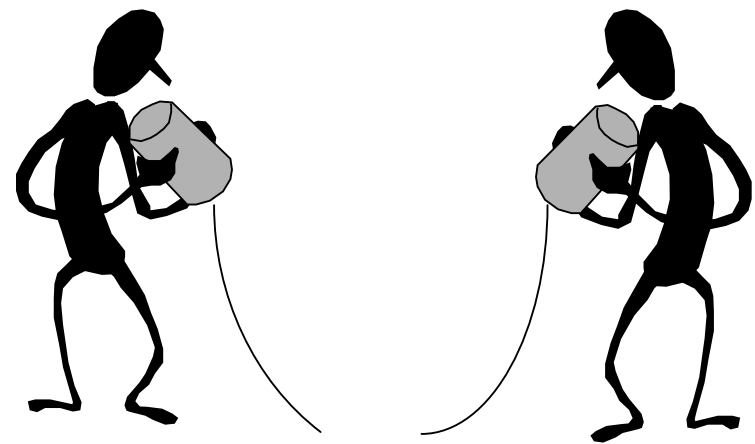
Common Data Formats

- GDSII Stream (polygon data)
- EDIF 2.0 Netlist Data
- JEDEC 3B Test Vector Format
- TSSI Test Format
- VHDL {IEEE 1076}
- Verilog HDL {IEEE 1364}



Data Interchange Media

- QIC6150 / 6250 / 6525 tar tape
- PC floppy disk
- DAT tar tape
- CR-Rom
- Zip Disk
- email
- 1/2" Magnetic tape



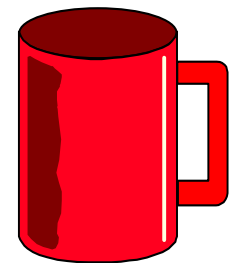
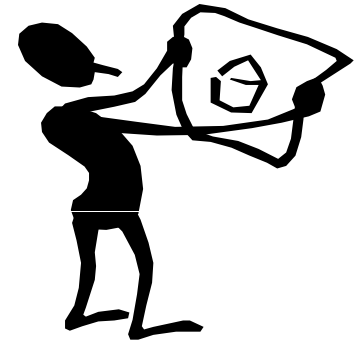
Code of Practice

- Honesty
- Understand REAL requirements
- Detailed knowledge of :
 - Design Tools
 - Relevant Technologies
 - Processing & Packaging Issues
 - Semiconductor Theory
- Adherence to Quality Standards
- Pragmatic & Creative approach
- Understanding of Cost sensitivities

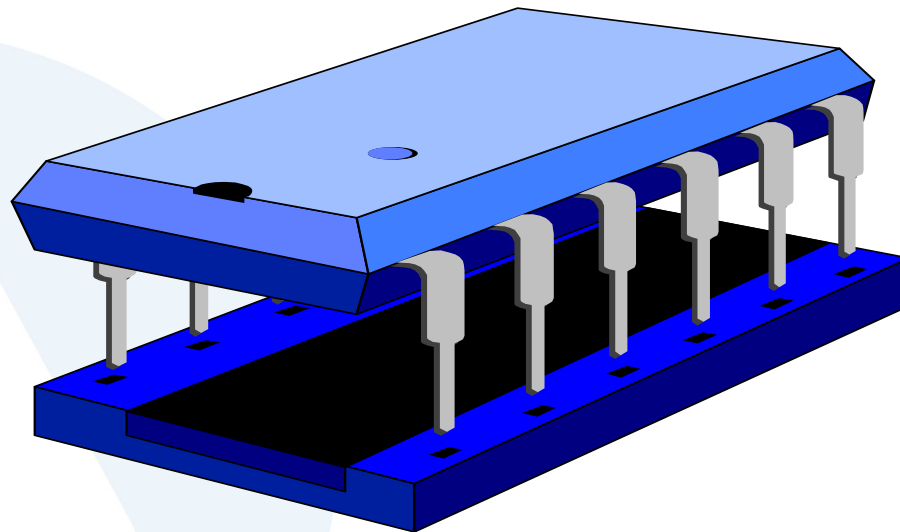


Preparation

- A Schedule or Work Plan
- A Specification would be nice !
- Accurate data
- Number of pins, types, etc.,
- Top Down or Bottom Up ?
- Special test needs, JTAG, LSSD etc.,
- Vendor, Technology & Library
- Relax A mug of hot coffee !



ASIC Technologies



Technical Options

- FPGA / PAL / PLD
- Gate Array
- Semi-Custom Array
- Field of Transistors
- Predesigned Base Array
- Full Custom
- Multichip or Hybrid



Fabrication Technologies

CMOS & SOS

BiPolar

BiCMOS

GaAs (III-V)

NMOS



Logic Families



CMOS & NMOS
TTL & DTL
RTL & HNIL
ECL, PECL, & CML
IIL

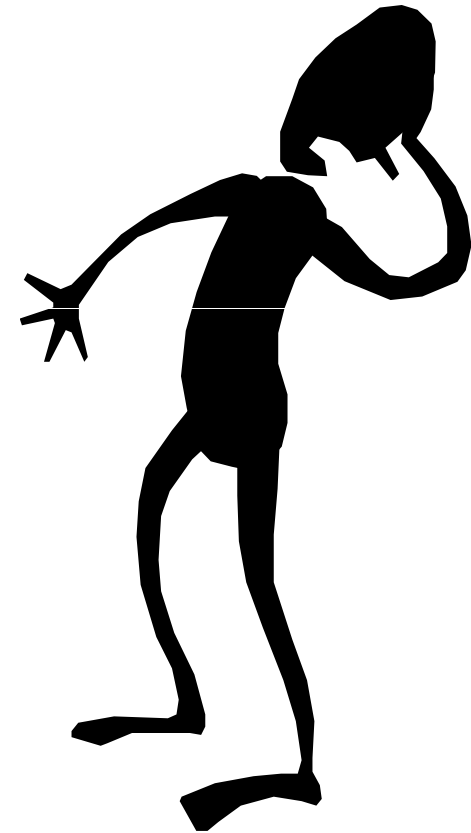
CMOS Technology

- ✓ Low Cost
- ✓ High Density
- ✓ Medium Speed
- ✓ Easily Interfaced
- ✓ Switch-Cap analog solutions
- ✓ Low Supply Current requirements
- ✓ Universal availability
- ✓ Shrinking Geometries
- ✗ Poor DC Stability
- ✗ Static & Radiation Sensitivities
- ✗ Poor Power Handling
- ✗ Poor High-Voltage Power Supply



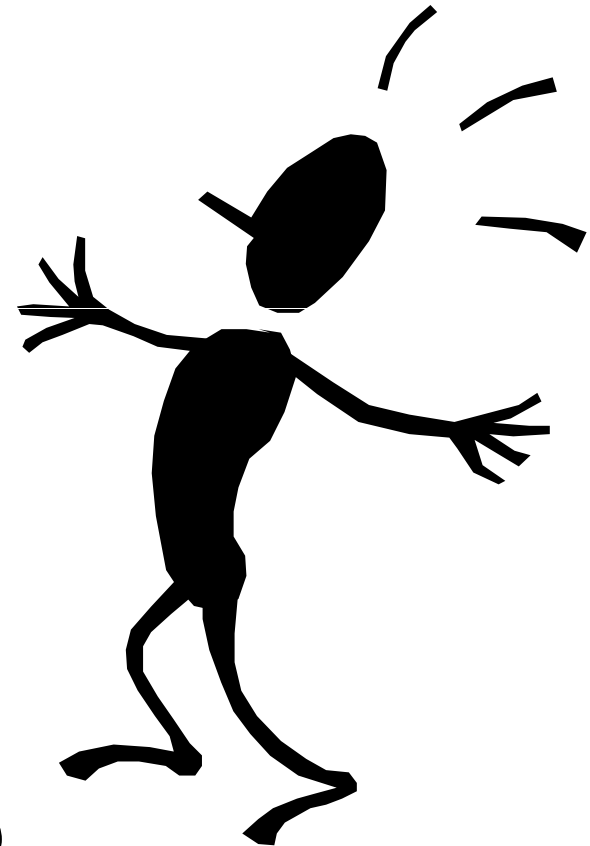
BiPolar Technology

- ✓ Very High Speed
- ✓ Accurate and Stable DC's
- ✓ Wide Power Supply Range
- ✓ Medium Cost
- ✓ Excellent High Power Capability
- ✓ Good Static & Radiation Immunity
- ✗ Power Hungry
- ✗ Low to Medium Density
- ✗ Limited Availability
- ✗ Closure of many Fab lines



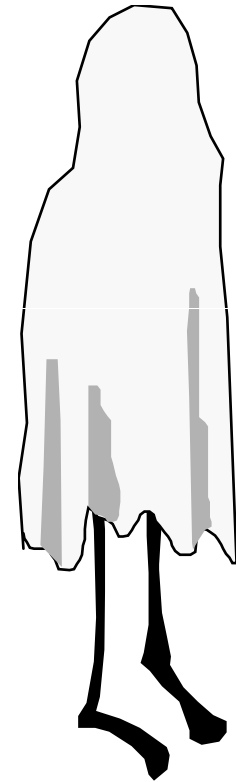
BiCMOS Technology

- ✓ Very High Speed BiPolar
- ✓ High Density CMOS
- ✓ Accurate & Stable DC's
- ✓ Acceptable Power Supply range
- ✓ Easily Interfaced
- ✓ Switched-Cap analog options
- ✓ Low to Medium Supply Current
- ✓ Good High Power Switching
- ✗ High Masking Costs
- ✗ High Manufacturing Costs
- ✗ Limited availability, but increasing
- ✗ Static & Radiation Sensitivities (as CMOS)



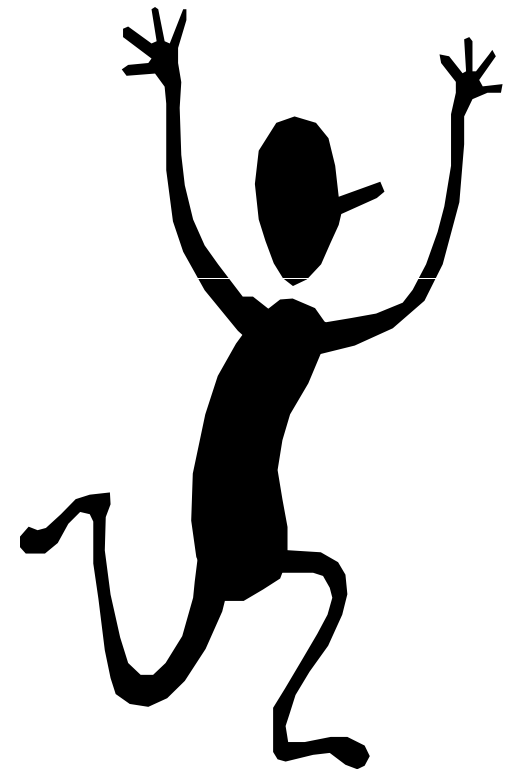
III-V Technologies

- ✓ Very High Speed
- ✓ Low RF Noise
- ✓ Medium Density
- × Mediocre DC Stability
- × Static & Radiation Sensitivities
- × Poor power handling capability
- × Very Expensive, high processing costs
- × Poor Thermal Stability
- × Very Limited Availability



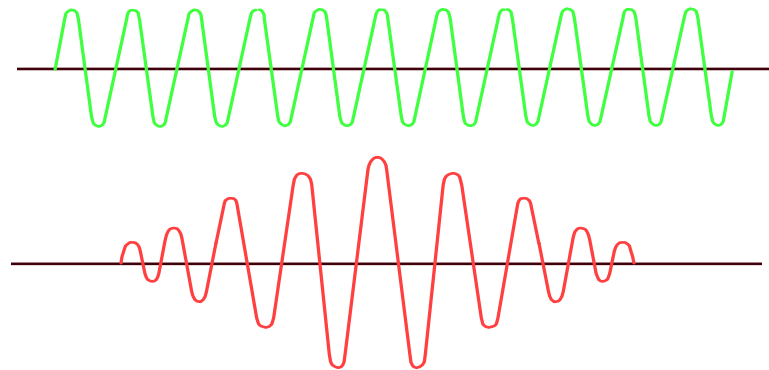
SOS-SOI Technologies

- ✓ Radiation Hardness
- ✓ Potentially faster than CMOS
- ✗ Very High Cost
- ✗ Very Limited Availability
 - ✗ Getting harder to find
- ✗ Static Sensitive
- ✗ Poor CMOS characteristics



Choosing Analog Technologies

- High Speed
- Low Noise
- Inherent Stability & Accuracy
- Voltage & Current considerations
- Costs

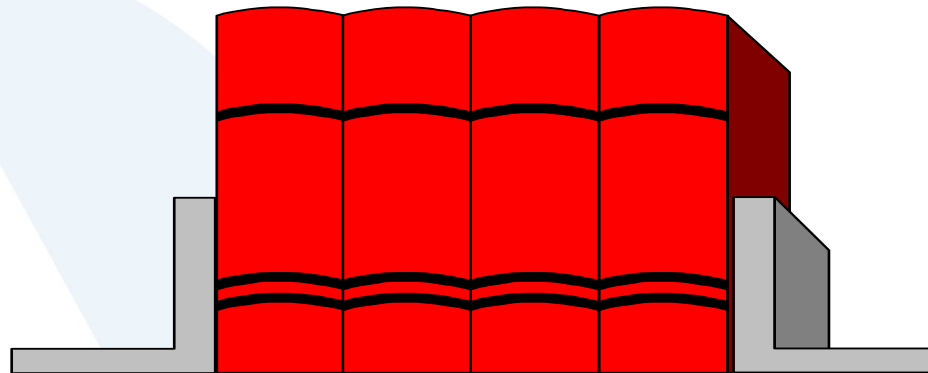


Other Considerations

- Hierarchy & Partitioning
- Methodology
- Packaging details
- Thermal requirements
- Operational requirements
- Life Time
- Mission criticality



ASIC Libraries



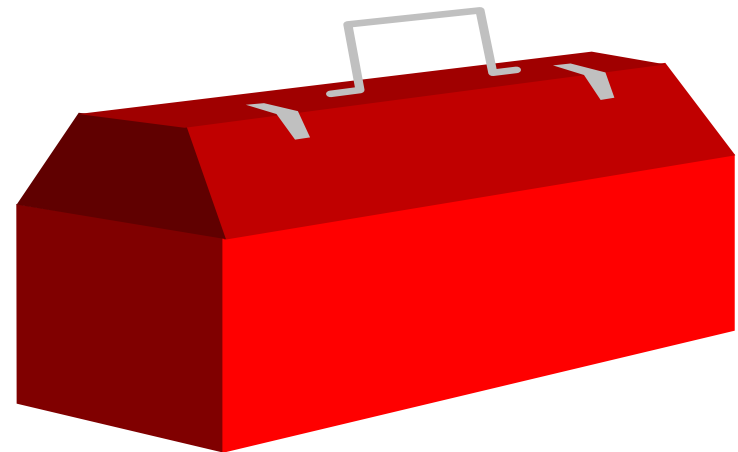
ASIC Library Contents

- Capability & Coverage
- Schema's
- Analog Models toleranced ?
- Digital Models min/typ/max ?
- Layout cells
- Geometries & DRC Rules
- Special ERC functions & Rules
- I/O Structure
- Chip Furniture details
- Authorized Documentation Pack



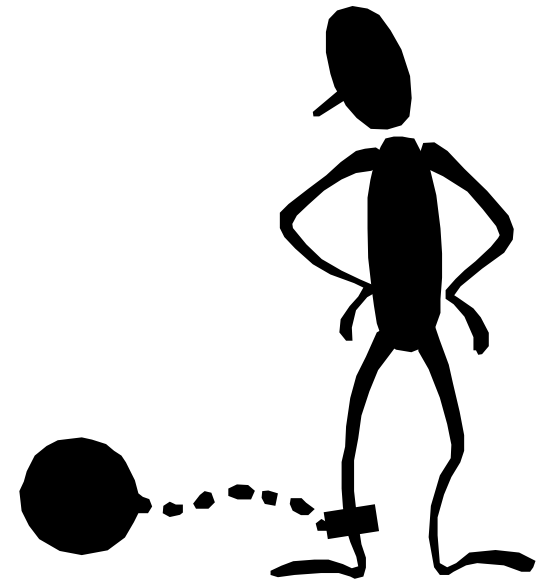
ASIC Components

- Diodes
- BiPolar Transistors
- MOSFET's & JFETS
- Resistors
 - range from 10R to 500K
 - Good Matching & Tracking (~1%)
 - Poor Absolute Tolerance (~25%)
- Small Capacitors
 - range from 0.1pF to 50pF
 - Fair tolerance (~5%)
 - Excellent Matching & Tracking
- Special Devices
 - Base Pinch resistors
 - Shottkey, Zener, Avalanche Diodes
 - Fusable Links, EEPROM cells
 - Photo/IR Sensitive cells



Technology Considerations

- 1, 2 or 3 layer metal (upto 7)
- 1 or 2 layer PolySi
- Low, Medium or High Poly Implants
- Number of Masks
- Special Mask Layers
 - Ni-Chrome Resistors
 - Substrate Contacts
 - Biased Epi Layers



Special Problems

- Current crowding
- I/O to Supply Pin ratio
- Nominal vs. Process Tolerances
- Model Accuracy
- Substrate Currents
- False or parasitic devices, complex structures
- Edge effects, strip-line effects, P1-M1-M2 caps.
- Package modelling & simulation
- Inaccurate back-extraction & simulation
- Poor absolute tolerancing
- Voltage dependancies
- Layout dependancies



Designing for Testability

- Initializing & Resetability
- Node Control & Observability
- Design redundancy, path replication
- Application vs. Test Methodology
- JTAG (**IEEE 1149.1**) boundary scan
- LSSD internal scan path
- Algorithmic testing
 - BIST, BILBO, PRBS, uCODE
- QTAG considerations

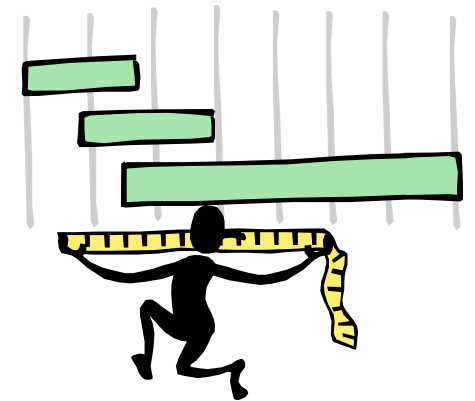
Designers Techniques

- Personal IPR & patents
- Detailed circuit knowledge of differing technologies
- DC & thermal stabilisation methods
- RF layout techniques
- Floor-planning methods, final die size reductions
- Specialist or homebrew tools



Do's and Don'ts

- Don't re-invent the Wheel !
- You can't make a silk purse from a sow's ear !
- Don't shoot at the moon, and then hit your foot (be realistic) !
- Do consider test !
- Do BACKUP everything regularly !
- Don't give away your IPR !





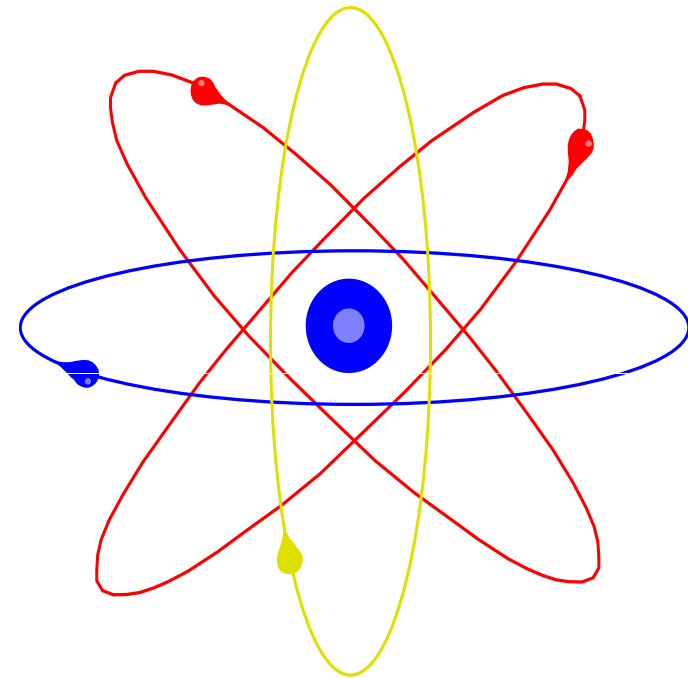
The ASIC Future

What's on the horizon ?

What problems can we foresee ?

Technology Push

- **Smaller Geometries**
 - Closing to the Atomic limits
 - Alternative technologies, improved III-V
 - Cu, SOI
- **Higher Pin Counts**
 - 1024+ horizon
- **Lower Voltages**
 - 5.0V to 3.3V to 2.0V to sub 1.0V!!!
- **Higher Speeds**
 - 1GHz+ on CMOS
- **New packaging techniques**
- **IEEE 1149.1 (JTAG) & Design for Test**
- **Larger Wafer Sizes**



... and the associated Problems

- Thermal Nightmare
 - P_{diss} climbing with die shrinking
 - Packages to minimize θ_{J+}
- Manufacturing Headaches
 - New Materials, Plastics, Attachment alloys
 - Socket Tooling
 - Bonders, Die placement & attachment, Pick & Place
 - Inspection & Diagnosis
- Test Problems
 - New Testers
 - Faster Test Rate + Increasing Vector Depth = Higher Tester Cost
 - New Test Methodologies
 - New Wafer and Device Handlers



Obsolescence

- Form-Fit-Function Replacement
- Redesign on 2-4 year cycle ?
- Automatic migration using VHDL ?
- Specialist Foundries with obsolete technologies
- J.I.T. vs. stock holding
- PAL/GAL replacement with alternative packaging
- Wafer and Die Banking
- Multipurpose-Multifunction ASIC's
- Smaller geometries, faster devices
- Reducing Supply Voltages, increasing supply currents

Design Routing

Design Flow
Simulation

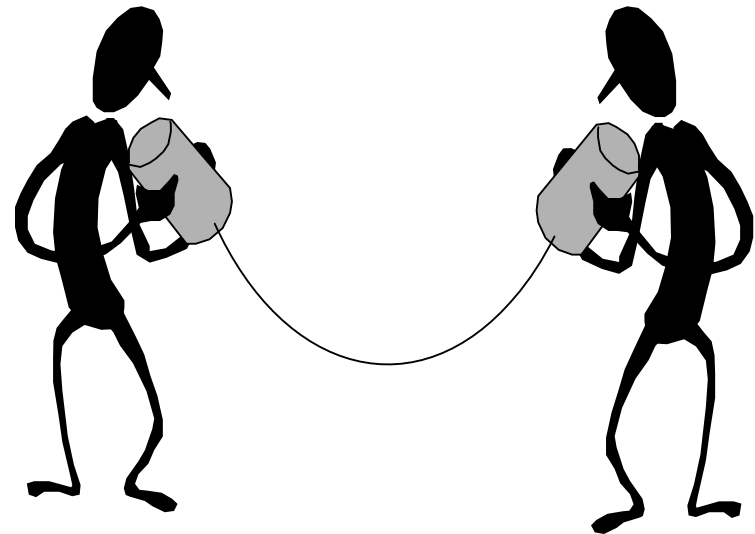


Design Flow

- Schematic Capture or VHDL Entry
- Pre-Layout Simulation
- Synthesis
- Layout
- DRC/LVS
- Back Annotation
- Post-Layout Simulation
- “Cutting the Tape”

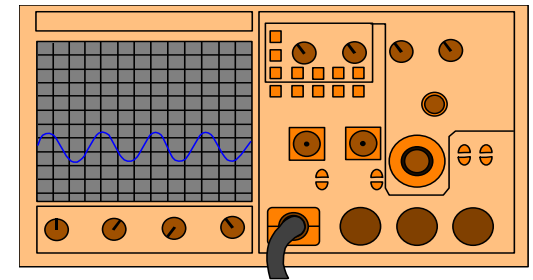
Quality Design Reviews

- DR0
 - Pre-order & quotation
- DR1
 - Initial kick-off and prelim. spec review
- DR2
 - Pre-layout simulation review
- DR3
 - Post-layout simulation review
 - Layout DRC, ERC & LVS review
- DR4
 - Prototype review
- DR5
 - Production review



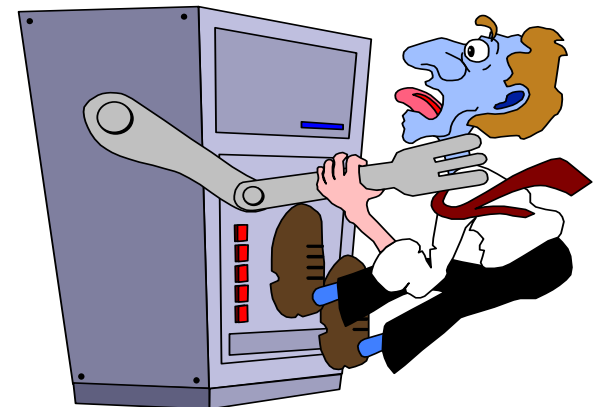
Analog Simulation

- Berkley 2G6 Spice Compliance
- Convergence problems & techniques
- Stability & Accuracy issues
- Frequency vs. Transient Analysis
- Min/Typ/Max Models
- Model Data Variance
- Monte Carlo analysis
- Model parameterisation & swept parameters
- Reviewing results, waveform viewers
- Arbitrary Waveform Format (AWF)



Digital Simulation

- VHDL or Verilog routes ?
- Other digital simulators
- Logic Models & Libraries - availability
- Time-mill or Event driven simulation
- Test Bench Design & Test Stimulii
- Time-sliced vs. Event wave data
- Using Test Vectors formats for result analysis
 - JEDEC 3B vector standard
- Fault Coverage & grading
- Limitations of waveform viewing
- Min/Typ/Max comparisons



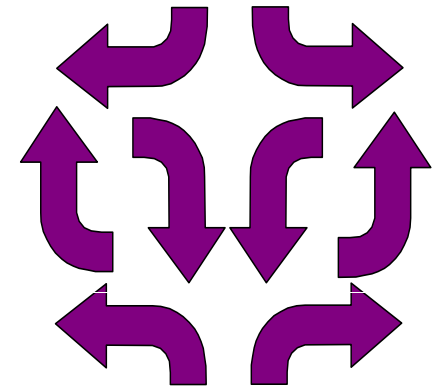
Mixed-Signal Simulation

- Use of twin simulators
- Defining Analog & Digital partitions
- Use of 1-bit A-D's & D-A's
- Realtime vs. Event driven
- Maintaining synchronicity between the Analog & Digital Simulators
- Typical Mix ... Spectre & Verilog-XL
- Other specialized simulators for :
 - RF & Microwave
 - Optics
 - Thermal Analysis
 - Test bench and tester



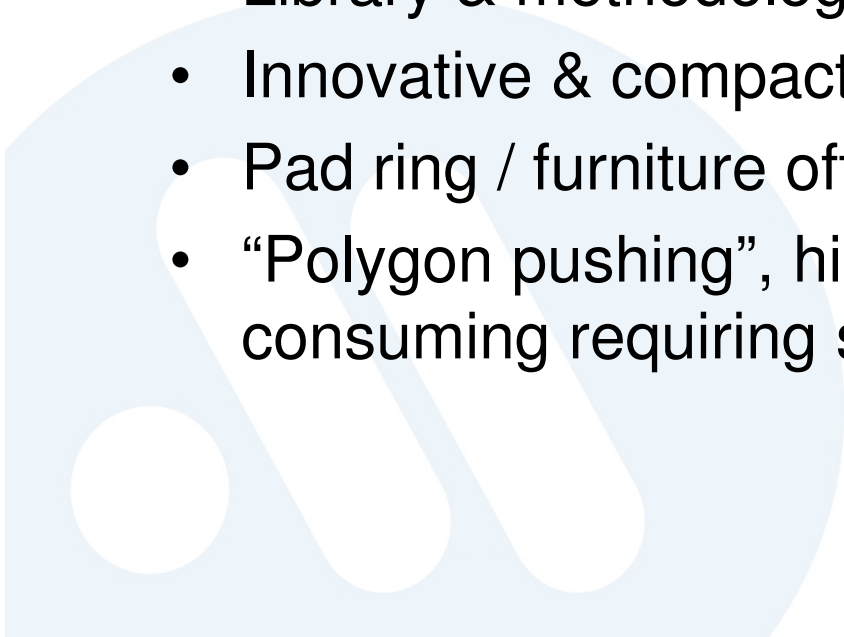
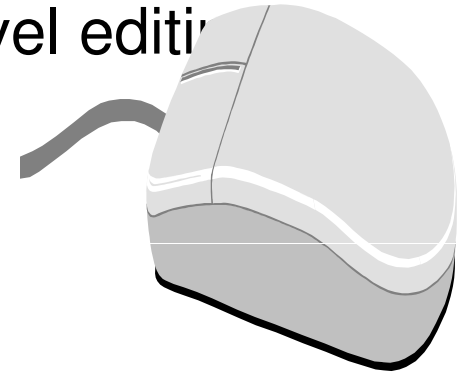
Automatic Layout

- Pin allocation must usually be predefined
- Floorplanner tool determines overall footprint
- Timing or Area driven layout options
- Clock chain should be pre-determined
- Individual MACRO pre-placement
- Auto Place & Route
 - Rip-up and re-try (slow)
 - Cooper & Chan routing algorithm
- DLM & TLM guided routing
- MACRO cell expansion for RAM/ROM
- Viable only for Digital cells at present



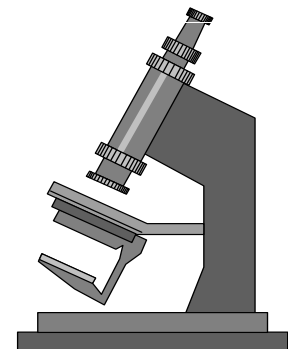
Manual Layout

- Fundamental device creation - device level editing
- Analog and special/unique circuitry
- Differential routing for ECL / CML
- Library & methodology creation
- Innovative & compact designs
- Pad ring / furniture often has to be handcrafted.
- “Polygon pushing”, highly intensive process, & time consuming requiring specialist engineering skills.



DRC & ERC Usage

- Polygon Extraction
 - Angular measurement
 - Radial segmentation
- Dimension Rules
 - Minimum widths and distances
 - Multilayer overlaps
 - Complex rules
 - Thermal relief rules
- ERC
 - Current densities & field strengths
 - Invalid connections (Power, shorted outputs)

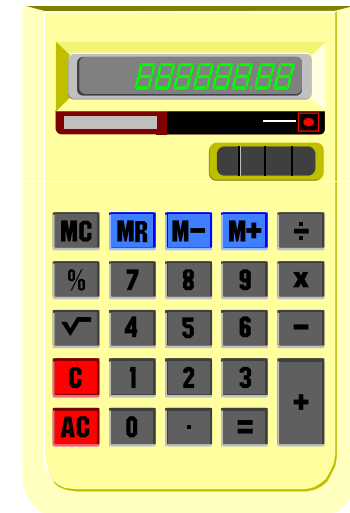


LVS & Extraction

- Obtains Electrical Data from Polygons
 - Designed 'R' & 'C' values from geometries
 - Parasitic 'L', 'C' & 'R'.
 - Edge effects, strip-line, lumped-element 'LCR'
- Active devices from vertical geometry
 - Determines NPNP junctions & active areas
 - Obtains MOS "W/L" characteristics
- Compares Extracted net-list against Schematic or Synthesised net-list
 - Simulatable net-list

From Simulation to Test

- Test strategy at design time
- ATPG & ATVG roles (and reality !)
- Test versus Application Vectors
- AWF files for Analog Testers
- File Conversion Methods
 - Simulator time slicing routines
 - External Post-processing
 - Vector file partitioning
- Additional data for test vectors
 - VOL, VOH, VOZ locations
 - Pin Formatting, Scrambling, DC Set-up & Timing Data



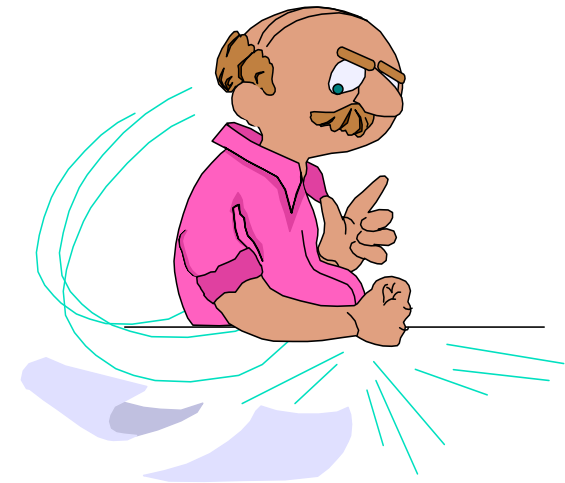
Information Routes

The Designers Output



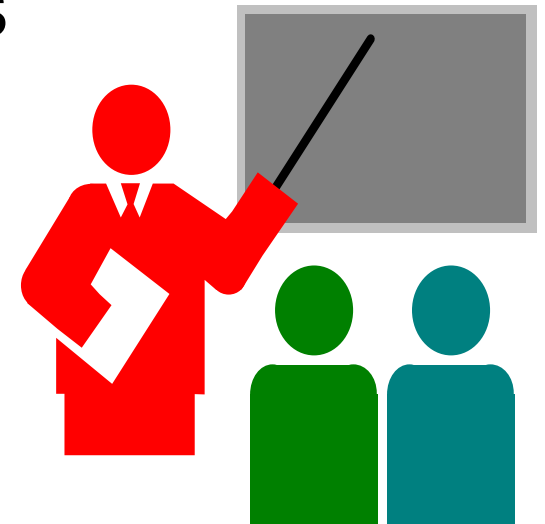
Who need what ? The Customer

- Detailed Schematics & notes
- Simulation results
- Manufacturing details
- Time Schedule
- The Quality Plan
- Test Results
- BSDL files ?



*Who needs what ?
The Sales & Quality Departments*

- Simulation & DRC/LVS Results
- “BOX FILE” data
- Time & Production Schedules
- Associated Costs
- Specification related data
- Qualification requirements
- Device characterisation



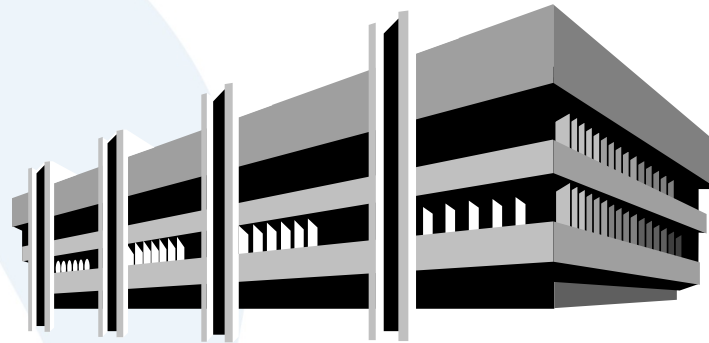
*Who needs what ?
The Mask Manufacturer*

- GDSII or CIF Tape
- DRC Rules used
- Reticule / Stepper sizing
- Dimensional information
- MASK OR'ing & AND'ing data



Who needs what ?
The Fabrication Plant

- Manufacturing Masks
- Process selected
- Geometrical information
- Any special process requirements

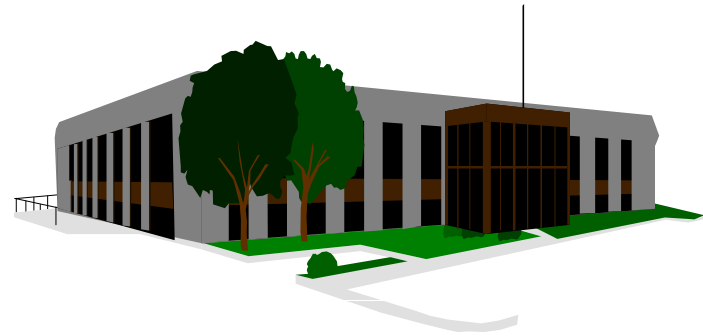


Who needs what ?
The Packaging House

- Die Size
- Package Style
- Device bond-pad layout & connection
- Marking & Branding details
- Chip carrier requirements
- If wafer bumping ...
 - UBM material etc.,

Who needs what ? The Test House

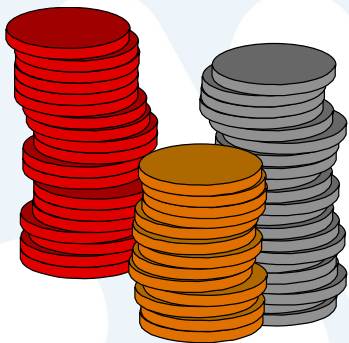
- Device Specification
 - Device Pin-out,
 - Package Style,
 - Bond-pad data
- Test Specification
- Functional test vectors
- Test Methodology
- Environmental Conditions
- Burn-In Circuit & details



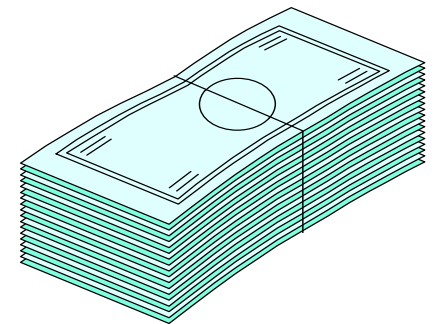
Project Costing

Typical European
ASIC

Development Costs



This is NOT a quote !!!



Typical Development Costs

- **Development NRE**
 - Design Effort, 7 weeks £20000
 - 15 Masks £15000
 - Test Development £ 5000
 - Test Hardware £ 4000
- **Commercial Production**
 - Prototype run, 25 off 4" wafer £10000
 - 40K probe test £ 3600
 - 20K packaging, 44 PLCC £ 9000
 - 20K final test £ 3000

Typical ASIC run costs

- Designer + Design Seat, per week £3000
- Mask manufacture, per mask £1000
- Wafer Costs, 4" £ 600
- Wafer Costs, 5" £ 750
- Wafer Costs, 6" £1000
- Plastic Packaging, per bond wire £ 0.01
- Test Costs, per second £ 0.05
- Test Hardware, incl. probe card £2000
- Test Software development, per week £3000