

Reliability concerns in modern Semiconductors

ENCASIT report # F6PE001A

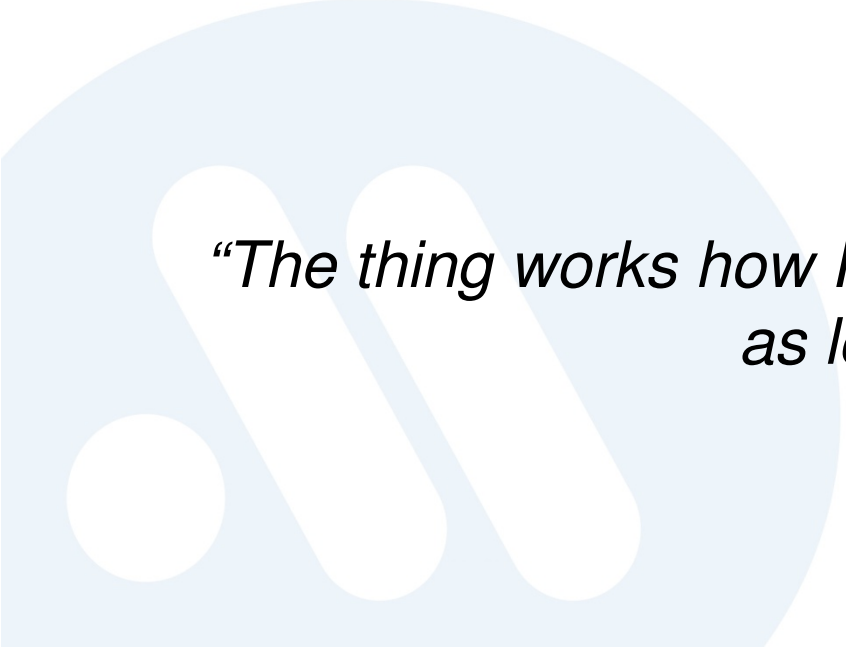
Alun D. Jones

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Reliability ?

The ability of a system or component to survive and acceptably function for a specified period of time within a given set of environmental parameters.

Or



“The thing works how I want and whenever I want, for as long as I want.”

Failure mechanisms in semiconductor devices

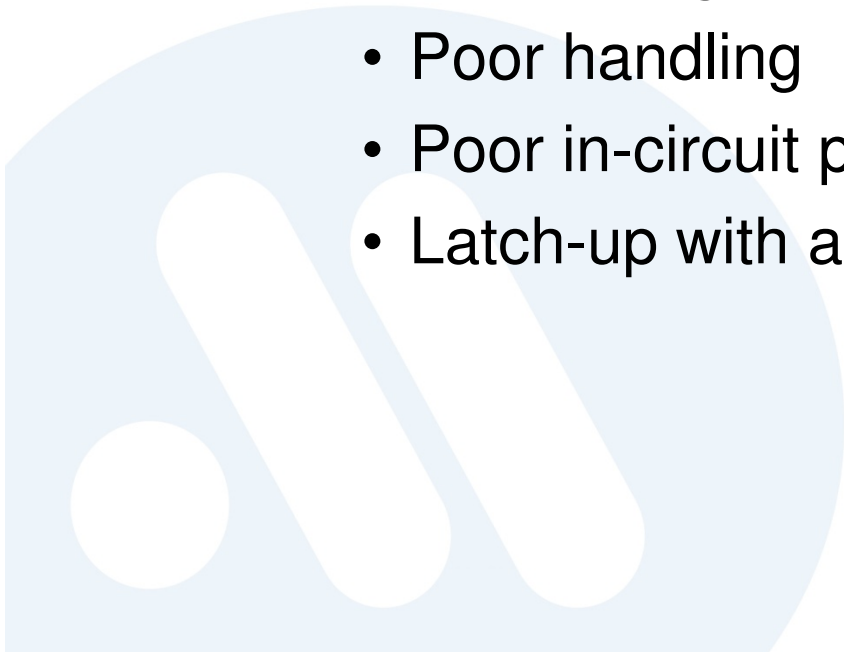
- Catastrophic Failures
 - Electro-mechanical & thermal
 - Electronic & electrical
 - Electro-chemical
- Hard but recoverable failures
 - Resettable, rebootable
 - Thermal
 - Power supply perturbation, external influences.
- Errors
 - Soft errors, aka. transient mistakes
 - Design “intolerance”

Catastrophic Failures

- **Electro-mechanical & thermal**
 - Thermal expansion & contraction
 - Mismatch & proximity of package material
 - Bondwire and bond attach
 - Piezo movement.
 - Attach mechanism
 - Mechanical vibration
 - Attach and assembly method
 - Bondwire material and length

Catastrophic Failures

- **Electronic & electrical**
 - Electrical overstress
 - External field influences, power supply faults
 - ESD damage
 - Poor handling
 - Poor in-circuit protection
 - Latch-up with an unforgiving power supply!

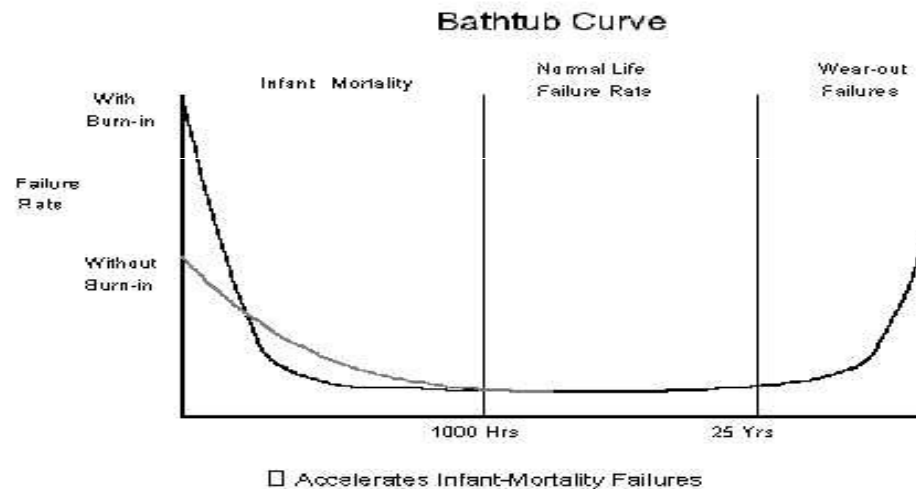


Catastrophic Failures

- **Electro-chemical** (main killers)
 - Metal migration
 - Movement of conductive material caused by an “electron wind”
 - Hot electron (carrier) effects (channel & substrate)
 - Charge trapping in gate oxide
 - Creation of interstitial states at Si-SiO₂ interface, degrading g_M and shifting V_T
 - Oxide / Nitride breakdown (rupture)
 - Dielectric breakdown due to voltage field stresses.
 - Other contamination residues
 - from processing etc.

Failures in Time (MTTF)

- Reliability with respect to time, the bath-tub curve.



$$MTTF = \int_0^{\infty} t \lambda_0 \exp(-\lambda_0 t) \delta t$$

The Arrhenius Equation

Known as the Arrhenius Equation, we use it to determine the Acceleration Factor, or **AF** in trying to predict failures from known mechanisms

$$AF = \exp(E_A/k * (1/T_N - 1/T_A))$$

AF	=	Acceleration factor
E_A	=	Activation Energy, in eV
k	=	Boltzmann's constant (8.62 * 10 ⁻⁵ eV/°K)
T_N	=	Normal junction temperature in °K
T_A	=	Accelerated junction temperature in °K

What it means ...

- Svante A. Arrhenius proposed this model for ionic chemical reaction rates in 1884. Nobel prize given in 1903.
- Not the only mathematical model used or available, certainly the most common used in predicting failure probability due to “chemical” effects. Many improved models now around.
- Demonstrates the exponential effect of temperature on accelerating the chemistry that we see as the root cause of failures within semiconductor devices.
- Using the Arrhenius equation, we can see that for an elevated junction temperature of 100°C (from T_N of 25°C to T_A of 125°C), we get an Acceleration Factor **AF** = ~353 assuming $E_A = 0.6\text{eV}$.
 - Or, put another way, 168 hours burn-in at 125°C equates to ~60,000 hours (7 years) operation at 25°C.

Activation Energy

- The Activation Energy, E_A levels in silicon semiconductors generally range from 0.3 to 1.2eV, dependant upon the failure mechanism mode. Each failure mode has it's own E_A value, mainly derived from experimental evaluation :

Failure Mechanism	E_A (eV)
Breakdown (Dielectric or Oxide)	0.25 to 0.4
Electromigration (Via/Contact)	0.8 to 0.9
Electromigration (Al)	0.5 to 0.7
Intermetallics	~ 1.0
“corrosion” (ionic reaction)	0.45
Surface contamination	~ 1.0
Charge Injection	1.3
Charge Loss (floating gate)	0.6 to 1.3
Charge Trapping	0.12 to 0.15
Hot Electron Trapping	~ -0.1

- It is quite common to see E_A quoted as between 0.6eV and 0.8eV, as a compromise value.

Technology marches on

Regardless !!!



The News ...

- What's good news
 - **All** stages of **all** processes are being steadily improved.
 - Knowledge of failure mechanisms and manufacturing issues is **better than ever**.
 - Manufacturing yields and productivity / function per cm² steadily increasing.
 - Chip's "*as cheap as chips*" ... falling costs as seen by the consumer.
 - Increasing functionality, Moore's Law still applying.
 - Increasing speeds, "decreasing" power consumption.
 - COTS ideal for the COTS market, with redesign & enhancement on a 18-30 month cycle.
 - Better design tools improve time-to-market cycles for "sexy" or novel products.
 - New, lower cost materials now becoming available.

And the News ...

- What's not so good
 - Manufacturers don't have to be so conservative in their designs.
 - Design for target market, not highest common denominator
 - Entry price into state-of-the-art technology increasing.
 - IC masking charges = exponential w.r.t. geometry
 - Fewer “players” left for pure foundry work.
 - Technology really is “off-shore”.
 - UK perspective, still some strong players in Europe.
 - Mass market expectancies being fed into “high-rel” market areas.
 - COTS is great for the COTS market, causes havoc with long-term “infrastructure” projects.
 - Cost of design migration now more weighted to layout & fabrication, not design.
 - Newer materials not necessarily ideal for high-rel or harsh environments.
 - But who cares ...

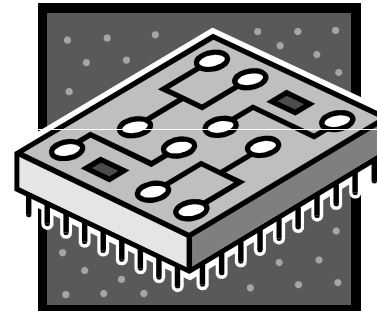
And more News ...

- Some knock-on effects
 - High reliability / conservative design silicon now left to a decreasing number of niche players.
 - Eastern block countries now offer some of the best solutions for older, more stable technologies.
 - FPGA usage increasing for small volume work.
 - Good device functionality migration
 - Poor electrical parametric or pin-pin compatibility
 - Changing power-supply requirements
 - Long term effects begin ignored
 - Military / Aerospace style requirements deemed irrelevant
 - Automotive seen as only stringent market by many players
 - Change in design strategy seen in many OEM's to cope with COTS market
 - Redesign accepted as being necessary throughout project life.

Current trends & developments.

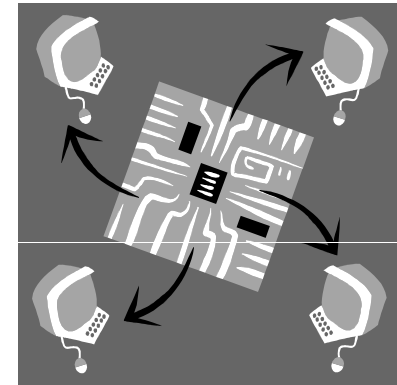
So, what's happening in ...

1. Design
2. Layout
3. Materials
4. Assembly
5. Packaging
6. Test
7. Procurement



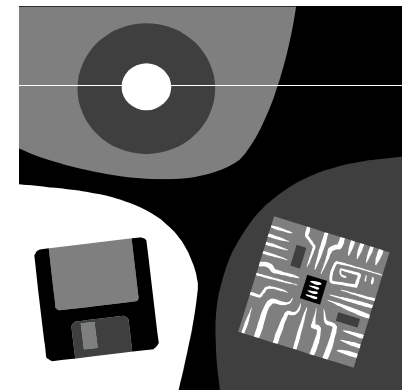
Current trends in Design

- Design to mission profile now “de-rigueur”
 - Not characterised for extended temperature ratings
 - Minimization of ESD structures
 - Design rules targeted for specific markets.
- Metal migration rules revised
 - Acceptable over-currents limits adjusted.
 - Limited operational lifetime ... guaranteed.
- Oxide/Nitride dielectric tolerance
 - Acceptable breakdown & leakage limits adjusted
- Pressure on any “pad-limited” design for shrink.
 - Moving of bond-pads into active regions
- Right first time methodology and toolsets.
 - Higher gate counts, faster gates
 - Design criticality, parasitics increasingly more important
 - Smaller margins of error
 - SoC & SiP becoming common goals, attention to design re-use & purchasable IP.



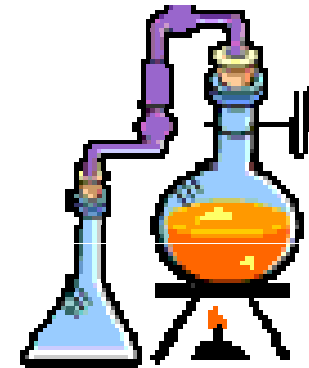
Current trends in Layout

- Geometry shrinkage
 - 90nm to 65nm to 25nm in 2-4 years. (DUV)
 - Voltage and internal leakage constraints.
 - Thermal & power limitations.
 - Newer processes only characterized for target markets
- Increasing interconnect layers
 - 7 layer metal common
 - Increasing TCE concerns
- Probe over passivation
 - Extended area for probing, not effecting bonding
- Loss of final outer “sealing-ring” of glassivation.
 - Saw widths decreasing
 - Cracks in passivation
- Highly automated design tools for automatic floor-planning
 - Still handcrafting RF & Analog circuits
 - Handcrafting for high density memory cells.



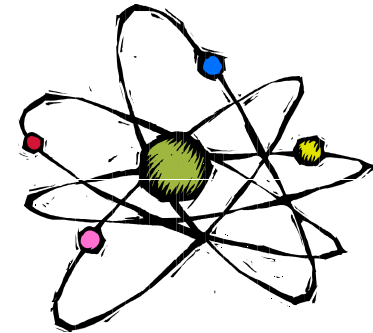
Current trends in Materials

- Copper interconnect
 - Improved conductivity
 - Long-term storage unknown
 - Advantage in having Cu-Cu-Cu attach throughout
 - Free from “intermetallic” issues
 - Corrosion issues
- Low-K dielectrics
 - “Softer” material, bonding issues.
 - Within-chip delamination of process layers after thermal cycling
 - Different Tco’s within die can limit mission usage.
- Reducing use of polyimide final passivation
 - Reliance on package to provide MSL3 (Moisture Sensitivity Level) @ 260C



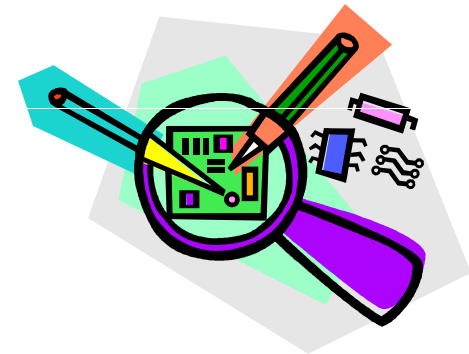
Current trends in Materials

- Silicon on Insulator (SOI) ... Dielectric separation
 - Reducing capacitance to substrate
 - Used to be SOS (Sapphire) Al_2O_3
 - Problems at interstitial boundaries
 - Often now SIMOX
 - Separation by **IM**plantation of **OX**ygen
 - Creates SiO_2 layer by heavy ion implant
 - Bonus in radiation tolerance
 - No parasitic NPNP structures in CMOS
- Other semiconductor “materials”
 - SiGe
 - Improved radiation tolerance thanks to higher doping levels.
 - Strained Silicon lattice base
 - III-IV materials (GaAs, GaP etc.,)
 - InAlP, InAlN type mixes for LED's & BandGap designed devices



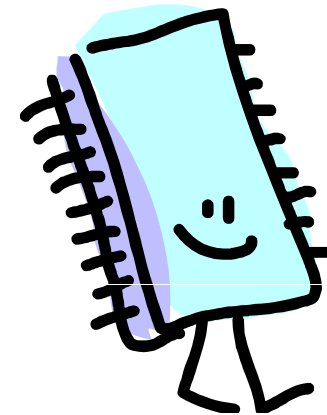
Current trends in Assembly

- Bondpad size & spacing decreasing ... fine pitch wire bonding
 - 125um – 100um – 60um is current spacing
 - 40um spacing by 2007
- Active circuitry under bondpad (known as BoA)
 - Damage to function by
 - Poor bonding
 - Thermal stresses
- Copper bondwires
 - Corrosion issues, oxidation & oxidization.
 - Incompatibility with older systems
 - New bonding systems required with unknown reliability
- Cleanliness
 - Plasma cleaning before bonding.
 - Automatic Optical inspection
 - Bonding in inert or reducing gasses



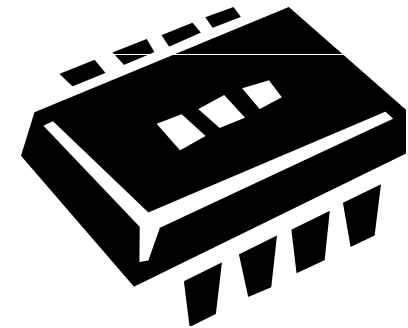
Current trends in Packaging

- Chip Scale or Wafer Scale packaging
 - Package approaches or equals die size
 - 1.1mm thin CSP in 2007
 - Package changes as die shrinks
 - Bump interconnect with surface re-routing
- Die, COB or COS used directly
 - Stacked die 3-5 high (9 seen already)
 - Automotive
 - Telecoms, mobile & static
- Bump, stud, ball, uPGA packaging
 - New packages arriving too fast for standardization to keep abreast of changes.
 - New inspection and repair techniques employed.
 - More reliance on auto-optical approaches
- Consideration for MEMs & Microsystems in package



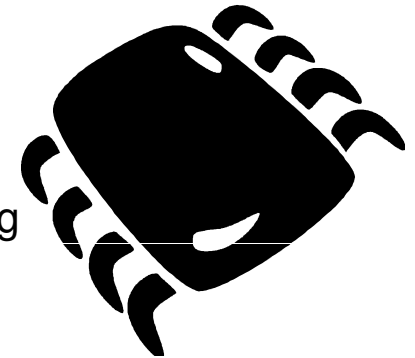
Current trends in Packaging

- Pb-free
 - Higher assembly temperatures
 - New lead finishes, new inspection procedures etc.,
 - Pressure on MSL levels, shop floor usage / active time
 - New packing materials & processes
 - Novel plastic packaging materials
- In-package antennae
 - WiFi, BlueTooth, ZigBee, 802.xxx
- Knock-on effect of high-volume users
 - Delivery mechanisms
 - Bandoleer, chip on tape, direct from wafer “pick ‘n place”.
 - Assembly techniques
 - Adhesive attach
 - Conductive adhesives
 - Non-corrosive and water washable fluxes
 - Placement and orientation accuracy (camera chips)



Current trends in Testing

- More “Guaranteed by Design” parameters
 - Fewer samples required
 - Characterised once at pre-production stage.
- PCM data more relied upon
 - Tamagochi product not tested
 - Major Taiwanese foundries no longer fully functionally testing
- Internal BIST/BILBO etc., sacrificed.
 - Excessive overhead & cost on cheap product.
- RF Testing now becoming more complex
 - RF components now becoming mainstream
 - Probing at + 2.4GHz.
- High cost of ownership of xx-VLSI testers
- Intelligent test limits
 - Achieving very low DPM's
 - PAT, IDDq, AIDDq techniques regularly employed
- Niche areas of Wafer-Level Burn-in and test etc.,



Current trends in Procurement

- Higher volumes direct from “Foundry to User”
 - Relationships between foundry & user excludes stockists and alternative customers.
- Foundries now selling on process and PCM spec’s
 - Some (very large) foundries now becoming “single market” suppliers.
- Some users now becoming as expert in foundry operation as the foundries themselves
 - Information flow increasing, under strict NDA’s
 - Die & wafer delivery
 - 3rd party intermediate processing services
 - Bump or balling
 - Chip / die tape and reeling

Current trends in Procurement

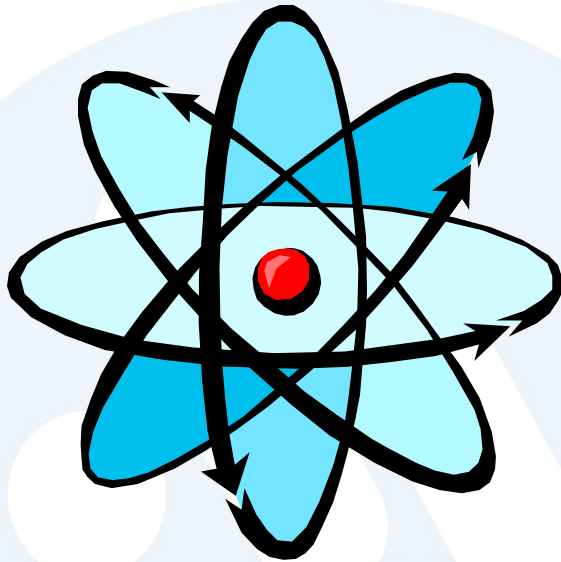
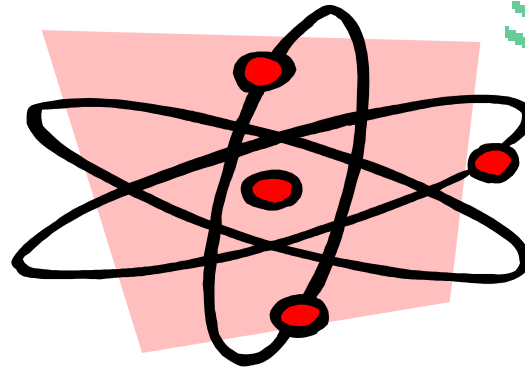
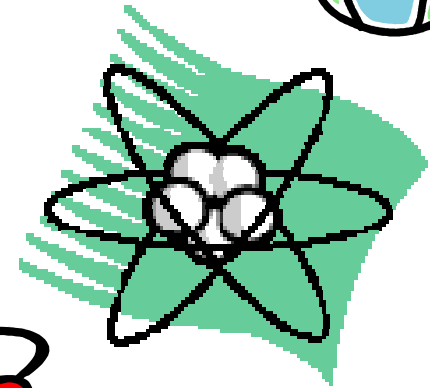
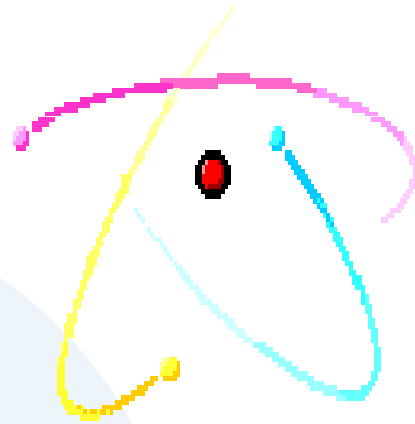
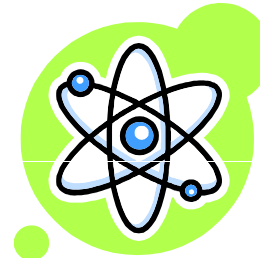
- Unique contracts
 - Fabs having to bend due to consumer “strength”
 - More liability being “flowed” down
- Zero DPM targeted for specific environments
 - Field failures taken ever more seriously
 - KGD becoming expected from suppliers
- Customer demands of design to application
 - Characterised for single markets
 - Limited lifetime expectancy.
 - Continuous pressure on cost reductions
- US & Europe still stronghold in “Mid-Rel” or “Hi-Rel” devices
 - More product is dropping from “Mid-Rel” to “Commodity”.
 - Increasing volumes are begin designed / manufactured / assembled in Far East.
 - Top end design still being done in US & Europe.

... the overall effects

- Smaller geometries == lower voltages & higher leakage currents
 - Lower voltages => smaller noise margins
 - Lower voltages => higher power supply currents
 - Smaller geometries => Increased SEU effects
- Design for specific “Mission Profile”
 - Not intended for operation outside given parameters.
 - high-rel or harsh environments only when specified.
- Denser packaging, smaller interconnect
 - Specialist packaging, package types quickly superseded.
- Increased functionality: SiP, SoC etc.,
- Fewer players in “open market”.
- Increased on-board thermal issues.
- Limited life expectancy
 - Regular / periodic redesign / product launch assumed



Radiation effects



Single Event Effects (Radiation)

- Mil-Aerospace has it as a known issue for the past 30 years
- Two main sources of particles ...
 - Thermal neutrons, energy $> 15\text{eV}$
 - High-energy cosmic particles : Neutrons, protons or muons... which cause reactions with Si & O₂
 - Leaving ionised pockets -> trapped charge
- Sea Level effect of 20 neutrons/cm²/hr now major concern for high density digital, mainly SRAM and soon to be Flash
- 5Km height yields around 7200 neutrons/cm²/hr
- Growing awareness from industrial and other “rel” products, not tamagochi.
 - No longer seen as “scare tactics” from the academics

Current classifications of SEEs

- **SEUs ... Soft Error Upsets**
 - The most common SEE to date, are generally regarded as transient upsets to data
- **SELs ... Single Event Latch-ups**
 - Normally destructive if not catered for or designed out.
- **SEFIs ... Single Event Functional Interrupts**
 - The sort of effect that causes infinite microcomputer program loops or lockouts.
- **SEBs ... Single Event Burnouts**
 - Destructive, usually by rupturing the gate oxides of individual transistors ... non-recoverable. Very rare, usually only seen in large, high-voltage power FETs.
- **SETs ... Single Event Transients**
 - More prevalent in smaller geometries, seen as a voltage / current spike that can effect data propagation.

Single Event Effects (Radiation)

- Effects are now regularly seen as single- or multiple-logic errors, initially in high density memories (such as SRAM).
- Current SEE sensitivity predictions for low voltage Flash look very poor.
- Package materials important, for low neutron emission.
- Memories will bring back error detection and correction (parity, hamming codes etc.,)
- Microprocessors and other logic may need detection correction.
- Use of multiple redundancy and voting systems may be needed.
- Tentative hope that even smaller geometries will become less sensitive, as active-area depth will also shrink.
- Refer to test method JESD-89
- *Don't always blame Microsoft if your PC crashes !!!*
 - *Sun recall of server workstations well publicised*
 - *Cisco Systems have SEE failures on it's 12000 series router line cards (RRP \$200K)*



Cosmic SEE Process sensitivities



Process	Application	Sensitivity
0.25um	Consumer	None
	Networking/Storage	None
	Aero/Mil	Memory/Logic
0.18um to 0.13um	Consumer	None
	Networking/Storage	Memory
	Aero/Mil	Memory/Logic
90nm	Consumer	Memory/Logic
	Networking/Storage	Memory/Logic
	Aero/Mil	Memory/Logic
65nm and below	Consumer	Memory/Logic
	Networking/Storage	Memory/Logic
	Aero/Mil	Memory/Logic

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BJT radiation effects

- Low dosage radiation effects on BJT's
 - BJT's usually considered hard for space / aerospace.
 - Generally neutron effects in the base creating electron-hole pairs.
- Main failure mechanisms
 - Observed as increase in Collector-Emitter leakage.
 - Results in gain reduction of wide-base BJT's
 - Narrow base RF transistors affected to a lesser extent.
 - Increased recombination sites mean that even parasitic BJT's degrade, (more sensitive to latchup).
- Issues being addressed
 - ELDRS ... Enhanced Low Dose Rate Sensitivity
 - More degradation shown at low dosage rates.
 - PETS ... Pre-Irradiated Elevated Temperature Stress
 - High temperature annealing can increase rad. Sensitivity.
 - HBT ... Hetero-Junction Bipolar Transistors
 - SiGe Base material etc., show improved hardness

***Do we have new reliability
issues ?***

You Decide!



Any Questions?



Just some other facts ...

- To make a 6" wafer with 0.18micron technology, it takes ...
 - around 2300 gallons of DI water
 - around 300KW hours of energy
 - and 3200 cubic ft of bulk gasses
- To make build a complete desktop PC, it takes ...
 - 240Kg of fossil fuels
 - 22Kg of chemicals
 - 1500Kg of water,
 - and contains over 2lbs of Lead (including the display)