

# *Obsolescence*

## *Component Emulation & Substitution*

*Alun D. Jones*  
*Technical Director*

[www.microSS.com](http://www.microSS.com)



*For Obsolescence, consider ...*

A light blue decorative graphic on the left side of the slide, consisting of a semi-circle at the top, a circle at the bottom left, and two vertical bars in the center, all within a larger light blue shape.

*The 3 **F**'s of Requirements  
&  
The 5 **R**'s of Solutions*

# *The Requirement*

- The **F**orm
  - ☞ Identical or Conforming Packaging
  - ☞ Matching the Footprint
  - ☞ Require to use the same board assembly techniques
- The **F**it
  - ☞ Specification
  - ☞ “Fit for purpose”
  - ☞ Same decoupling ?
- The **F**unction
  - ☞ What goes on inside the Chip
  - ☞ Living with the application
  - ☞ Same pin-out & power supplies

## *And the Options for replacement*

- **Obsolescence Solutions, the 5 R's**
  - **Re-Package**
    - Calling off from die stocks
  - **Replace with similar product**
    - COTS, spec. change, up-screening
  - **Re-Invent,**
    - using MCM / Hybrid techniques
  - **Refit**
    - PAL/PLD copying device function
  - **Re-Design,**
    - using ASIC solutions

## *The **FORM** - packaging*

- Package styles can go out of fashion
  - packages not being banked as yet
  - not seen as major issue to date
- Easy work-arounds for existing packages, but ...
  - “canning” will become an issue
    - reduced capability
  - look at current packages (CSOP, uBGA), can they be so easily mimicked ?

## *The **FIT** - specification*

### **Silicon is silicon !**

*Fine in theory but not all foundries ...*

- provide the same service
- have the same technology
- characterise for Hi-Rel usage
- provide libraries for Hi-Rel.
- offer external access
- offer limited batch runs
- believe that you exist ...

*or want to get involved at all !*

## *The **F**UNCTION*

- Matching the Function
  - Identical operational performance
  - Mimicking the bugs
  - Watching for unspecified Areas
  - Where necessary, characterise original parts
- The threshold of **PAIN**
  - *You can't always get what you want ...*
  - Non-identical silicon technologies
    - Otherwise we wouldn't have obsolescence !
  - Best fit ... not perfect fit.

## *So what is going obsolete ?*

- The Device
  - The Silicon
  - The Package Style or Form
  - The speed grade, temperature grade or dash option
- The Tester
  - Tester and Test interface / adapters
  - Test Software
- The Data
  - Crumbling tapes
    - Old 1/2" mag. CALMA tapes
    - No tape readers
  - Obscure data formats
    - QIC (non-TAR formats)
  - Poor data archive, only checked when needed, not when put away .
- The Knowledge
  - The tricks and traps that made the original thing work.
  - Making Engineers Obsolete is not a Smart Thing !!

## *Supply Issues*

- Business generally too small to attract many foundries
- Fewer “available” technologies
  - We often want / need :
    - Bipolar
    - Higher Voltages (*and 5V is high to some people*)
    - Slower speeds
    - 1 wafer !!!!
    - Military / Industrial Grade Silicon
    - Traceability
  - We can often only get :
    - CMOS or BiCMOS
    - Decreasing Voltages
    - Higher speeds
    - At least 25 wafer MOQ
    - Commercial Silicon
    - Minimal Paperwork

## *“The Bottom Line”*

Solution Providers must...

- Adjust the customers expectations
  - to what can realistically be achieved with ...
    - the available technology,
    - his small quantity and
    - his minuscule / derisory budget
  - to what he can expect ...
    - from you,
    - from the foundry and
    - from the package supplier
  - and at what cost
  - and within what timescales
- If the customer still can't accept reality
  - Know when to **“WALK AWAY”** !

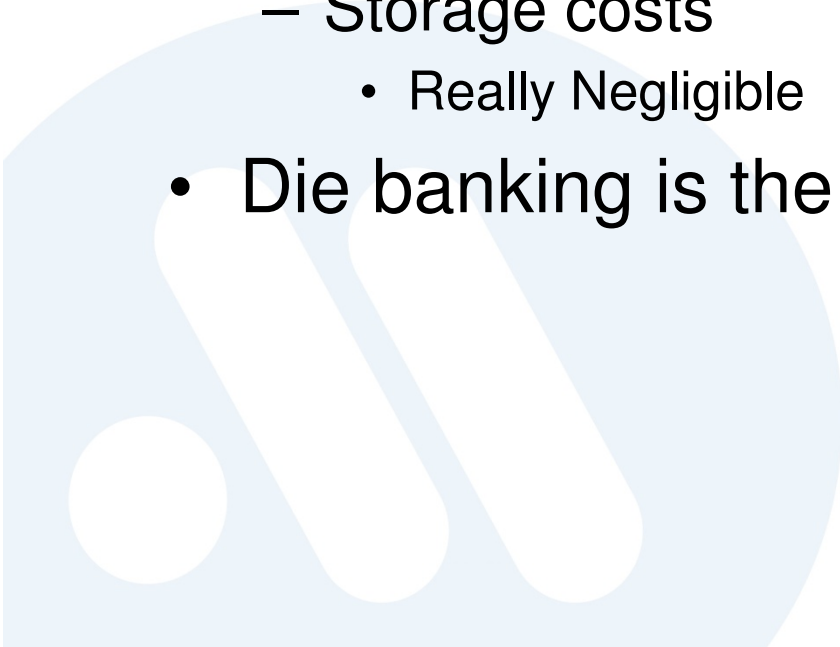
*Above all, be honest*

## *Re-Package*

- Easiest and simplest solution, provided ...
  - Die stocks are still available
    - Assumes someone has had a bit of foresight !
    - *Luck or judgement ?*
  - Packages are available
    - Most still are, but Canning is getting more expensive.
  - The information & knowledge is still there
    - Paper still has it's uses !
  - The Assembly equipment is still running
    - Generally catered for ... not seen as an issue yet.
  - The Test equipment/software/hardware is still alive
    - Starting to become an issue with older ATE & parts.
    - Test programs can generally be converted ... at a cost !

## *Dispelling the Myth*

- Die banking is **NOT** expensive
- Cost of ownership is down to ...
  - Purchase of die
    - Ascertain real needs, quantity, yield etc.,
  - Storage costs
    - Really Negligible
- Die banking is the **CHEAPEST** alternative



# *Replacement*

- Generally a fair option ...
  - Perform technical appraisal
  - Match technical specifications
    - *be tolerant of minor changes*
  - Run through Engineering Trials
  - Sample production batch runs
  - Upscreen parts where necessary
- ... as long as it's done properly
  - older parts have no direct replacement
  - if it now works ...
    - *think about banking what you can get now*

## *Replacement - using COTS*

- *When purchasing Commercial items, you are accepting the T's & C's of the commercial world ...*
  - *Die's may shrink*
  - *Package styles go obsolete*
  - *Foundries may change*
  - *Longevity of product supply is questionable*
  - *Quality of product often an unknown quantity*
  - *Design rules not necessarily established for long-term product reliability.*

## *Replacement - COTS Scenario*

- Manufacturer “A” once made :
  - Military Grade of component “X”
  - Commercial Grade of component “X”
- Manufacturer “A” now only makes :
  - Commercial Grade of component “X”

*Okay to purchase Commercial & up-screen ?*

- Manufacturer “A” has many foundries making component “X”, using different lines, different technology, different die etc.,
- Actual foundry that made Military grade now obsoleted original fab/test equipment used, no inspection facilities etc.,
- **BUT Commercial supply still not a problem !**

## *Re-using “used” stock*

- Re-living or re-validating old components from
  - Old inventory
    - *Check in the engineers “drawer” !*
  - Old boards
    - Vapour-phase desoldering, component lift.
- Components can be “pre-aged”
  - Generally only a few can be salvaged
  - Device history can be suspect
  - Rework etc., can cause damage.

# *Re-Invent*

## Getting smart with substrates

- Good success with digital parts
  - Signal and Power re-routing
  - Interposer dielectric issues
- MCM techniques well understood
  - Beware of yield influencing issues.
- Can overcome “silicon” problems with ...
  - additional passives
    - decoupling,
    - impedance matching
    - external resistor & capacitor absolute accuracy
  - extra chip's
    - delay elements
    - additional functionality
  - additional connections / terminals
    - test connections
    - programming
- **Test fault coverage and substrate testing is paramount**

## *Re-Fit with PLD's*

- The Programmable Logic option ... some issues
  - Can't match supply conditions
  - Won't meet parametric specification
  - Can't match pin-outs
    - Interposer connector may be used for re-scrambling
    - PLD usually has more pins, used for programming etc.,
  - Newer technologies == faster parts, *speed is always an issue*
  - Often very high cost piece parts.
- **BUT**
  - The correct mixture of PLD's and substrates can work
  - after a fashion ...
  - Reasonably fast turnaround
  - Can be the lowest cost option !
  - *You gotta know watcha doing*

## *Re-Fit with masks*

- Mask Conversion & Re-Use
  - Obtain masks (GDSII) and process rules
    - assume that original manufacturer agrees !
    - \$\$\$\$ passes hands
  - Select appropriate process
  - Process characterisation and mapping
    - Expensive use of Process Engineer
  - Layer-Layer conversion to new process
    - Layout Engineers time (semi-automatic)
  - Mask re-sizing to accommodate new rules
  - Mask Manufacture
    - Expect to pay at least \$1000 / mask ... 14 + masks ?
- BUT
  - I've never seen it done on a low cost budget !!

# *Re-Design*



The ASIC Option

# *Old 2 New ASICS*

- Requirements before commencing a **DIGITAL** design ...
  - Original Procurement Specification
  - Current Test Specification
  - Schematics, Netlists, or VHDL / Verilog
  - Test Vectors (or Test Bench for VHDL / Verilog)
    - needed to corroborate Schematic / Netlist.
  - Data on the original silicon Library
  - Any notes, documents or details from those originally involved in the first design.
- **Gotcha's**
  - Unknown revision of silicon.
    - Additional “tweaks” made ... multiple spins
  - Documentation not matching working devices (*very common*)
  - Undocumented requirements (*extremely common*).

# *Supply Issues - Design Houses*

- Design house - Foundry Relationships
  - Design house “buffers” foundry from small volume users and most technical interrupts.
  - Design house becomes major customer of foundry, often gets preferential treatment.
  - Design house can consolidate designs (*sometimes*) on MPW runs.
- Can be compromised by the End Customer
  - Not committing to production volumes.
  - Delaying project.
  - Wanting only “Engineering” runs.
    - only wanting a minimal number of devices
  - Attempting to go direct to foundry.
  - Demanding fast turn through foundry (*generally with no cost*)
    - delays in customer commitment don’t help (*sanitised version*) !

**Remember....**

**you may want to use this Design House & Foundry again !**

## *Design “Languages”*

- VHDL / Verilog
  - “Ideal” for technology transfer
  - **BUT** watch for
    - Timing constraints
    - Poorly written code
    - Non-existent device libraries
  - Too many poor designs “scrape” by.
  - Foundries generally prefer Verilog
  - European designers generally prefer VHDL

# *Circuit Diagrams*

- Schematics
  - A **MUST-HAVE** for Analog designs
    - Transistor sizes often needed in older bipolar designs
  - Require **ALL** schematic sheets
  - Difficulty with reading complex designs
    - older dye-line drawings
    - A0 sheets reduced to A4 !
      - Or even smaller
  - Limited to ~25K gates
    - *brain fries above this for random logic*

## *Got any Devices, Guv ?*

- Use of original devices ...
  - Characterise for
    - DC Parametric values
    - Timing
    - Pin characteristics
  - Check “under the bonnet”
    - determining fabrication technology
    - for unusual geometry
    - match transistor sizes, resistor lengths
    - peculiar bonding or assembly

# *Summary of DC Parametrics*

- Power supply requirements
  - Decoupling, range & tolerance
- Inputs & Outputs
  - Requirements
    - Thresholds, Drives, Slew / Skew, Loading
  - Types
    - CMOS, TTL, RTL, ECL, other oddities
- DRC rules on bond pad requirements

# *Summary of AC Parametrics*

- PSU
  - Decoupling, PSRR
- Timing
  - Critical paths,  $t_{PD}$ 's,  $t_{SU}$ ,  $t_{HD}$ , etc.,
  - Clock path skew, race conditions
- Design rule speed
  - Too fast ?, too slow ?
  - Hand tweak'd original design ?

# *Supplies ! - Supplies !*

- Power Supply Issues
  - Decoupling
    - Is existing decoupling going to be enough ?
    - Multiple bond wires for core-periphery ?
  - PSU range / tolerance
    - We're designing for Military / Aero
    - Do I need 10% supplies ?
  - Does the PSU rely upon the ASIC load ?
  - Supply environment
    - Is supply okay for new silicon ?
  - PSRR ?
    - Are we going to hurt the supply ?
  - Power connections already defined
    - Breaking foundry design rules ?

## *In one pin ...*

- Inputs (digital)
  - Input type
    - Schmidt's
    - Pull Up's / Down's
    - TTL / CMOS / ECL / CML compatible
  - Loading & Leakage
    - Does application rely upon loaded inputs ?
    - Default Logic level when open ?
    - Asymmetric leakage actually required ?
  - VIH/VIL Threshold levels
  - Dependence on VCC/VDD ?
  - Special cases ?

## *... and Out the next !*

- Outputs (digital)
  - Drive capability and characteristics.
  - I/O Leakage requirements
  - Slew and Skew specifications ... if known.
  - Rate limiting ?
  - JTAG / SCAN requirements
    - *can be larger than the components real function.*
  - Restrictions on Power Supply Connections
    - Limitation of I/O vs. Power pins
    - Supply pin / Output pin placement already fixed !

# *It's all in the t... t... t... timing*

- Timing
  - Is new silicon too fast ?
    - Older designs could be sloppier in race timing issues
    - Analog silicon can “hoot” due to poor board layout or application.
  - Is new silicon too slow ?
    - Handcrafted designs for critical paths
  - Critical tPD's
  - Clock skew throughout design
    - was it intentional ?
    - what type of clock tree do I need now ?
  - Impact on application.
  - Effect of change in package type / style

# *Analog designs ... Ouch !*

- Everything as for digital, including :
  - Information / Data, such as ...
    - Transistor geometric sizes
    - Passive component limits and tolerances
    - Original design rules, breakdowns and parasitics
  - Layout information required
    - GDSII or CIF data very helpful, layer data essential
    - *Even taking a 12' ruler to old plots !!*
  - Application Circuit is a MUST !
    - Board layout data also can be helpful
    - Info on decoupling, hi-speed traces etc,.
  - Very old technologies
    - unusual devices / topography / characteristics
    - no hard and fast design rules
    - high value capacitors ~ 300pF
    - unique processing, eg. NiCr, Fusing, HiBV<sub>CE</sub>
  - TREAT ECL / CML / PECL as ANALOG !

## *Re-Design Benefits*

- Creates good buffer stock of devices
  - Die banking
- New Design technology offers ...
  - Modern processing
  - Up-to-date testing
    - Automatic test program generation
    - Automatic test vectors
    - Better test coverage
  - Easier “upgrade” path in future
  - Can solve “gotcha’s” in original design.
- Once successful, encourages future use.
  - Assured longevity promotes design re-use
  - Customer more confident on Re-Design route.

## *For new designs*

- Consider good archive data **NOW** !
  - Paper, CD, Mag. Tape, etc.,
- “Future-proof” yourself ...
  - VHDL / Verilog design methodologies
  - Buy plenty of Wafers
    - Die Bank if necessary (applied foresight, not luck)
  - If Digital, archive all data
  - If Analog/MS, archive all data, plus ...
    - Layout (GDSII, CIF)
    - Simulation (Test benches, analog set-ups)
  - Grab **ALL** the designer’s notes !!

## *In summary*

- The Requirement ... the 3 **F**'s
  - **F**orm, package and footprint
  - **F**it, specification and environment
  - **F**unction, what it does, and how it does it.
- The Solutions ... the 5 **R**'s
  - **R**e-Package the die
  - **R**eplace with similar product
  - **R**e-Invent, using substrate technologies, etc.,
  - **R**e-fit using PLD's or masks
  - **R**e-Design ... the ASIC solution

## *The 5 R's for the solution provider....*

- **R**ealistic
  - provide more than one solution, offer good value for money
- **R**eactive
  - reacting to give one or more timely cost-effect solutions
  - customers must allow time for proper CONSIDERED answer.
- **R**eputable
  - be known for capability in all redesign methodologies
  - and succeeding !!!
- **R**elationship
  - The supplier/customer technical interface is *CRUCIAL*
  - Foundry relationship secures the future
- **R**igorous
  - Thorough engineering solutions by healthy collaboration
  - Engineering and Quality teams working together to provide comprehensive checking and documentation

**MicroSS Components strive to excel in all these criteria, to become a worldwide leader in component emulation and substitution, providing engineered solutions to many equipment manufacturers.**

