

# The Environmental Screening Can o' Worms

## The Microcross Components Guide to Environmental Test and Screening

The How's and Why's of environmental testing and screening ...

- *What's the best screening routine for my "XYZ" part?*
- *What do the individual tests tell me about my part?*
- *Am I doing enough?*
- *Or am I going overboard on my testing?*
- *What ARE the available options?*

# Environmental Test and Screening

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## **Why do we environmentally screen parts?**

Environmental screening is intended to determine whether a particular device or batch of devices can survive in a given environment, for a known period of time. Additionally, this type of screening is used to remove devices that have imperfections during design and/or manufacture that would lead to premature failure in its intended working environment.

## **Tests discussed**

### **Temperature related tests**

- Dynamic Burn-in
- High Temperature Operating Life (HTOL)
- Stabilisation bake
- Data retention bake
- Temperature cycle assessment and test
- Thermal shock
- Highly Accelerated Stress Test (HAST)
- Autoclave and 85/85 tests

### **Mechanically related tests**

- Particle Impact Noise Detection (PIND)
- Gross and Fine leak
- Centrifuge
- Mechanical vibration

### **Electrically related tests**

- Solderability
- Latch-up assessment
- ESD assessment and test
- Thermal testing

## **Dynamic Burn In**

### **How**

Device is dynamically operated at elevated temperature, generally 125°C, for 168 hours or 1000 hours.

### **Why**

Accelerates the majority of real-life failure mechanisms. 168 hours operation at 125°C equates to over 7 years normal operation at 25°C. Refer to the later section on “Why Burn In” for further details and data.

## **High Temperature Operating Life (HTOL)**

### **How**

Device is dynamically operated at elevated temperature, generally 125°C, for an extended period, often upto 8000 hours.

### **Why**

Accelerates the majority of real-life failure mechanisms. To predict the reliability of the product type.

## **Stabilisation Bake**

### **How**

Device is stored, unbiased, at elevated temperature, generally 125°C or 150 °C, for typically between 24 and 48 hours.

### **Why**

Performs final “annealing” of device, enhancing any contamination during final manufacturing process. Note that stabilization bake is generally not performed on “regular” logic or analog parts nowadays.

## **Data retention bake**

### **How**

Unbiased device storage for upto 1000 hours at 125°C or 150°C, similar to stabilisation bake.

### **Why**

Accelerates failures in Flash or EEPROM type technologies, generally associated with charge leakage from the storage element, equating to data loss of the device. Note that this applies mainly to memory storage devices that claim data retention.

## **Temperature Cycle Screen**

### **How**

Devices are cycled, in air or inert gas, from cold to hot, generally from -65°C to 150°C, for a small number of cycles, generally between 5 and 10, with a specific rate of change of temperature.

### **Why**

Eliminate manufacturing defects prone to failure due to thermal expansion.

## **Temperature Cycle Assessment**

### **How**

Devices are cycled, in air or inert gas, from cold to hot, generally from -65°C to 150°C, for a large number of cycles, upto 1000 cycles, with a specific rate of change of temperature

### **Why**

Determine the reliability of the product when exposed to regular temperature cycles. This test exaggerates the stresses that can occur from power-cycling, revealing any weaknesses caused by mismatch of thermal expansion between die and package.

## **Thermal Shock Assessment**

### **How**

Devices are mechanically transferred from one temperature extreme to the other extreme in as fast a time as practical

### **Why**

Thermal shock highlights thermo-mechanical incompatibility from mechanical expansion / contraction, often caused by the selection of incorrect materials or processing.

## **HAST- Highly Accelerated Stress Test**

### **How**

Devices are subjected to both high temperature (~130°C) and humidity (~85% RH) in a pressurised environment, with or without electrical bias.

### **Why**

Accelerates ionic contamination and corrosion within die/package interface and device leads. Tests for ingress of moisture in plastic packages Note that this is only applicable to plastic packages.

## **Autoclave**

### **How**

Devices are subjected to high temperature (121°C) and saturated humidity (100% RH) under no bias conditions

### **Why**

Accelerates ionic contamination and corrosion within die/package interface and device leads. Tests for ingress of moisture in plastic packages Note that this is only applicable to plastic packages.

## **Temperature Humidity Test - 85/85 Test**

### **How**

Devices are subjected to high temperature (~85°C) and humidity (~85% RH) with or without electrical bias.

### **Why**

Accelerates ionic contamination and corrosion within die/package interface and device leads. Tests for ingress of moisture in plastic packages. Note that this test only applicable to plastic packages.

### **PIND - Particle Impact Noise Detection**

#### **How**

Device is subjected to both mechanical vibration and shock in alternating cycles, with a sensitive microphone attached listening to sounds from within internal hermetic cavity

#### **Why**

To detect extraneous particles within a hermetic cavity, which may impact and embed upon the active die surface, thereby interfering with the device operation.

### **Gross Leak**

#### **How**

Cavity packages are subjected to a high-pressure gas, such as air or a fluorocarbon, and then placed in a high-temperature inert liquid and monitored for emerging bubbles indicating gas egress from the package.

#### **Why**

To ensure hermeticity of a cavity package.

### **Fine Leak**

#### **How**

Cavity packages are subjected to a high-pressure inert gas, such as Helium, and then placed in a mass-spectrometer to detect minute traces of the gas. Helium is often used due to its small molecule size.

#### **Why**

To ensure hermeticity of a cavity package.

### **Centrifuge**

#### **How**

Devices are placed in a centrifuge and subjected to angular acceleration, typically upto 30,000 G's.

#### **Why**

Tests the mechanical stability and survivability of the final assembly, including die attach and bond-wires, especially to extremely high perpendicular acceleration forces.

### **Vibration (shake, rattle 'n roll) Assessment**

#### **How**

Devices are placed on a mechanical vibration jig, that subjects the device to a number of vibration cycles, ranging from 1-, 2- and 3-axis shock, and frequency swept vibrations.

**Why**

Tests the mechanical stability and survivability of the final assembly, including die attach and bond-wires, including susceptibility to resonant vibrations.

**Solderability Assessment****How**

Devices are solder-dipped under worst case conditions, and then visually examined.

Various techniques, including the measurement of surface tension, are often employed.

**Why**

Ensures the ability of the device to be used in a normal manufacturing environment. Note that this will become more prevalent as various Pb-free solder mixtures are used with differing fluxes.

**Latch-Up Assessment****How**

High voltage pulses are sent to each I/O pin on a device, and the supply current is monitored to detect latch-up, in accordance with JEDEC 57.

**Why**

Modern CMOS technologies inherently have a self-regenerative NPNP structure which, under certain circumstances, can

cause destructive supply currents to flow, known as "latch-up". This test assesses the protection mechanisms employed to prevent the occurrence of "latch-up"

**ESD Testing and Assessment****How**

A purpose-built ESD tester is used, forcing a human or machine body-model discharge to each device pin in turn for a number of cycles, then analysing each pin with a V-I curve trace to detect ESD damage.

**Why**

Devices, especially employing CMOS technology, are susceptible to I/O pin damage caused by electro-static discharge. This test assesses the ESD protection.

**Temperature Screening****How**

Devices are electrically tested at both temperature extremes.

**Why**

To ensure compliance to the data-sheet specification, and to ensure correct operation in application. Note that different failure mechanisms or device marginality can be observed and highlighted during these tests.

## Why Burn-in semiconductor devices ?

Ask any “old” engineer what makes a semiconductor device fail after a period of operation, and he’ll list stress (voltage and temperature) and time as being the main causes. His answer will be generally borne out of experience and “gut-feeling”, rather than from any mathematical derivation, but he happens to be right about the weaknesses of semiconductors.

Reliability here is the probability of a semiconductor device performing its intended function adequately for a given period, under specified conditions. Thus the reliability of a semiconductor device is a direct function of both stress and operating time.

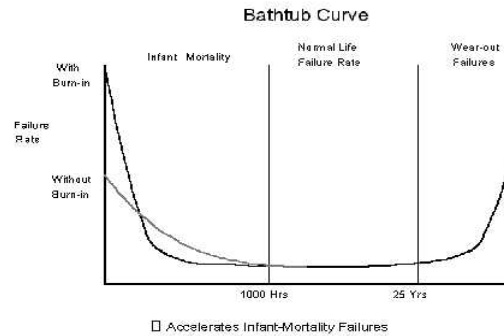
This probability (or reliability) of survival can range from zero (no chance of survival) to one (no chance of failure), and modern semiconductor devices are manufactured to such rigorous standards that reliability figures of 0.9999 to 0.999999 are often achieved. As these figures approach unity, it is more normal to quote the probability of failure (1 - probability of survival), often as parts-per-million, or PPM.

The failure rate is therefore the rate at which failures occur on devices surviving a specific time, and commonly the number of failures per billion operational hours is

given, often known as FIT’s (Failure In Time).

## The “bathtub” curve

The usual graph of device failure versus time takes the shape of a bathtub curve, with the “infant mortality” period starting from initial operation, and decreasing as time goes on. At the end of the infant mortality, the next period is characterized as having a low and almost constant failure rate over a long period of time, known as the “normal operation” period. Towards the end of operational life, the “wear-out” period starts, this time characterized by a slowly increasing failure rate.



## The Arrhenius Equation

So we can determine and predict failure rates, it is necessary to enhance the causes of failure, thus accelerating the occurrence of failures. Higher stress levels that those found under normal operating conditions are employed, and the most commonly used failure acceleration parameter is junction temperature, often coupled with supply voltage. There exist a number of mathematical models to quantify the relationship between the acceleration of failure rates and junction temperature, the most common is use being that model proposed by Svante A Arrhenius for chemical reaction rates.

Known as the Arrhenius Equation, we use it to determine the Acceleration Factor, or **AF**.

$$AF = e^x,$$

$$\text{where } x = E_A/k (1/T_N - 1/T_A)$$

$$(8.6172 * 10^{-5} \text{ eV/}^\circ\text{K})$$

**T<sub>N</sub>** =Normal junction temperature in  $^\circ\text{K}$

**T<sub>A</sub>** =Accelerated junction temperature in  $^\circ\text{K}$

Using the Arrhenius equation, we can see that for an elevated junction temperature of 100 $^\circ\text{C}$  (from **T<sub>N</sub>** of 25 $^\circ\text{C}$  to **T<sub>A</sub>** of 125 $^\circ\text{C}$ ),

**AF** = Acceleration factor

**E<sub>A</sub>** =Activation Energy, in eV

**K** =Boltzmann's constant

This Acceleration Factor (**AF**) can then be used to determine a certain probability failure at a specific time **t<sub>x</sub>** at temperature **T<sub>N</sub>**, compressing that time to **t<sub>x</sub>/AF**, by operation at the accelerated temperature **T<sub>A</sub>**.

The Activation Energy, **E<sub>A</sub>** levels in silicon semiconductors generally range from 0.3 to 1.2eV, dependant upon the failure mechanism mode. Each failure mode has it's own **E<sub>A</sub>** value, mainly derived from experimental evaluation, here are some typical values:

Failure Mechanism	E <sub>A</sub> (eV)
Breakdown (Dielectric or Oxide)	0.25 to 0.4
Electromigration (Via/Contact)	0.8 to 0.9
Electromigration (Al)	0.5 to 0.7
Intermetallics	~ 1.0
"corrosion"	0.45
Surface contamination	~ 1.0
Charge Injection	1.3
Charge Loss (floating gate)	0.6 to 1.3
Charge Trapping	0.12 to 0.15
Hot Electron Trapping	~ -0.1

we get an Acceleration Factor **AF** = ~353, or, put another way, 168 hours burn-in at 125 $^\circ\text{C}$  equates to ~60,000 hours operation at 25 $^\circ\text{C}$ .

It is quite common to see  $E_A$  quoted as between 0.6eV and 0.8eV, as a compromise value.

## **Conclusion**

Using elevated temperature, we can simulate the first “normal” seven years of operational use in just over one week. This burn-in of the semiconductor device moves the reliability point on the bathtub curve away from the “infant-mortality” period and into the “normal operation” period, and by subsequent testing these “early-life” or “infant-mortality” failures can be removed.

## The Arrhenius Equation

So we can determine and predict failure rates, it is necessary to enhance the causes of failure, thus accelerating the occurrence of failures. Higher stress levels that those found under normal operating conditions are employed, and the most commonly used failure acceleration parameter is junction temperature, often coupled with supply voltage. There exist a number of mathematical models to quantify the relationship between the acceleration of failure rates and junction temperature, the most common is use being that model proposed by Svante A Arrhenius for chemical reaction rates.

Known as the Arrhenius Equation, we use it to determine the Acceleration Factor, or **AF**.

$$AF = e^x,$$

$$\text{where } x = E_A/k (1/T_N - 1/T_A)$$

<b>AF</b>	=	Acceleration factor
<b>E<sub>A</sub></b>	=	Activation Energy, (in Ev)
<b>k</b>	=	Boltzmann's constant (8.6172 * 10 <sup>-5</sup> eV/°K)
<b>T<sub>N</sub></b>	=	Normal junction temperature (in °K)
<b>T<sub>A</sub></b>	=	Accelerated junction temperature (in °K)

This Acceleration Factor (**AF**) can then be used to determine a certain probability failure at a specific time **t<sub>x</sub>** at temperature **T<sub>N</sub>**, compressing that time to **t<sub>x</sub>/AF**, by operation at the accelerated temperature **T<sub>A</sub>**.

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Using the Arrhenius equation, we can see that for an elevated junction temperature of 100°C (from  $T_N$  of 25°C to  $T_A$  of 125°C), we get an Acceleration Factor  $AF = \sim 353$ , or, put another way, 168 hours burn-in at 125°C equates to  $\sim 60,000$  hours operation at 25°C.

## Conclusion

Using elevated temperature, we can simulate the first “normal” seven years of operational use in just over one week. This burn-in of the semiconductor device moves the reliability point on the bathtub curve away from the “infant-mortality” period and into the “normal operation” period, and by subsequent testing these “early-life” or “infant-mortality” failures can be removed.

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