

Linear Systems replaces discontinued Siliconix U402 with LSU402

The U402/ LSU402 is a Low Noise, Low Drift, Monolithic Dual N-Channel JFET

The LSU402 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The LSU402 features a 5-mV offset and 10- $\mu\text{V}/^\circ\text{C}$ drift. The LSU402 is a direct replacement for discontinued Siliconix U402.

The hermetically sealed TO-71 & TO-78 packages are well suited for military applications. The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

U402 / LSU402 Applications:

- Wideband Differential Amps
- High-Speed, Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES

LOW DRIFT | $V_{GS1-2}/T| = 10\mu\text{V}/^\circ\text{C}$ TYP.

LOW NOISE $e_n = 6\text{nV}/\text{Hz}$ @ 10Hz TYP.

LOW PINCHOFF $V_p = 2.5\text{V}$ TYP.

ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature -65°C to +150°C

Operating Junction Temperature +150°C

Maximum Voltage and Current for Each Transistor – Note 1

- V_{GSS} Gate Voltage to Drain or Source 50V

- V_{DSO} Drain to Source Voltage 50V

- $I_{G(f)}$ Gate Forward Current 10mA

Maximum Power Dissipation

Device Dissipation @ Free Air – Total 300mW

MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$ V_{GS1-2}/T $ max.	DRIFT VS. TEMPERATURE	10	$\mu\text{V}/^\circ\text{C}$	$V_{DG}=10\text{V}$, $I_D=200\mu\text{A}$ $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$
$ V_{GS1-2} $ max.	OFFSET VOLTAGE	10	mV	$V_{DG}=10\text{V}$, $I_D=200\mu\text{A}$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	50	60	--	V	$V_{DS} = 0$ $I_D = 1\text{nA}$
BV_{GGO}	Gate-To-Gate Breakdown	± 50	--	--	V	$I_G = 1\text{nA}$ $I_D = 0$ $I_S = 0$
TRANSCONDUCTANCE						
Y_{fSS}	Full Conduction	2000	--	7000	μmho	$V_{DG} = 10\text{V}$ $V_{GS} = 0\text{V}$ $f = 1\text{kHz}$
Y_{fS}	Typical Operation	1000	--	2000	μmho	$V_{DG} = 15\text{V}$ $I_D = 200\mu\text{A}$ $f = 1\text{kHz}$
$ Y_{fS1-2}/Y_{fS} $	Mismatch	--	0.6	3	%	
DRAIN CURRENT						
I_{DSS}	Full Conduction	0.5	--	10	mA	$V_{DG} = 10\text{V}$ $V_{GS} = 0\text{V}$
$ I_{DSS1-2}/I_{DSS} $	Mismatch at Full Conduction	--	1	5	%	
GATE VOLTAGE						
$V_{GS}(\text{off})$ or V_p	Pinchoff voltage	-0.5	--	-2.5	V	$V_{DS} = 15\text{V}$ $I_D = 1\text{nA}$
$V_{GS}(\text{on})$	Operating Range	--	--	-2.3	V	$V_{DS} = 15\text{V}$ $I_D = 200\mu\text{A}$
GATE CURRENT						
$-I_G$ max.	Operating	--	-4	-15	μA	$V_{DG} = 15\text{V}$ $I_D = 200\mu\text{A}$
$-I_G$ max.	High Temperature	--	--	-10	nA	$T_A = +125^\circ\text{C}$
$-I_{GSS}$ max.	At Full Conduction	--	--	100	μA	$V_{DS} = 0$
$-I_{GSS}$ max.	High Temperature	5	5	5	μA	$V_{DG} = 15\text{V}$ $T_A = +125^\circ\text{C}$
OUTPUT CONDUCTANCE						
Y_{OSS}	Full Conduction	--	--	20	μmho	$V_{DG} = 10\text{V}$ $V_{GS} = 0\text{V}$
Y_{OS}	Operating	--	0.2	2	μmho	$V_{DG} = 15\text{V}$ $I_D = 500\mu\text{A}$
COMMON MODE REJECTION						
CMR	$-20 \log V_{GS1-2}/V_{DS} $	95	--	--	dB	$V_{DS} = 10$ to 20V $I_D = 30\mu\text{A}$
NOISE						
NF	Figure	--	--	0.5	dB	$V_{DS} = 15\text{V}$ $V_{GS} = 0\text{V}$ $R_G = 10\text{M}$ $f = 100\text{Hz}$ $\text{NBW} = 6\text{Hz}$
e_n	Voltage	--	20	--	nV/Hz	$V_{DS} = 15\text{V}$ $I_D = 200\mu\text{A}$ $f = 10\text{Hz}$ $\text{NBW} = 1\text{Hz}$
CAPACITANCE						
C_{ISS}	Input	--	--	8	pF	$V_{DS} = 15\text{V}$ $I_D = 200\mu\text{A}$ $f = 1\text{MHz}$
C_{RSS}	Reverse Transfer	--	--	1.5	pF	

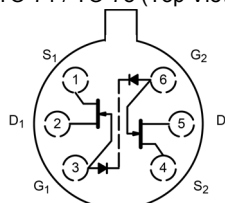
Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

U402 / LSU402 in TO-71 & TO-78
U402 / LSU402 in PDIP & SOIC
U402 / LSU402 available as bare die

Please contact Micross for full package and die dimensions

TO-71 / TO-78 (Top View)



P-DIP / SOIC (Top View)

