

## Linear Systems replaces discontinued Siliconix U401 with LSU401

The U401/ LSU401 is a Low Noise, Low Drift, Monolithic Dual N-Channel JFET

The U401 is a high-performance monolithic dual JFET features extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. This series has a wide selection of offset and drift specifications with the U401 featuring a 5-mV offset and 10- $\mu\text{V}/^\circ\text{C}$  drift.

The hermetically sealed TO-71 & TO-78 packages are well suited for military applications. The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

### U401 / LSU401 Applications:

- Wideband Differential Amps
- High-Speed, Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

### FEATURES

LOW DRIFT	$ V_{GS1-2}/T  = 10\mu\text{V}/^\circ\text{C}$ TYP.
LOW NOISE	$e_n = 6\text{nV}/\text{Hz}$ @ 10Hz TYP.
LOW PINCHOFF	$V_p = 2.5\text{V}$ TYP.

### ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)

#### Maximum Temperatures

Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C

#### Maximum Voltage and Current for Each Transistor

$-V_{GSS}$	Gate Voltage to Drain or Source	50V
$-V_{DSO}$	Drain to Source Voltage	50V
$-I_{G(f)}$	Gate Forward Current	10mA

#### Maximum Power Dissipation

Device Dissipation @ Free Air – Total	300mW
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### MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$ V_{GS1-2}/T $ max.	DRIFT VS. TEMPERATURE	10	$\mu\text{V}/^\circ\text{C}$	$V_{DG}=10\text{V}$ , $I_D=200\mu\text{A}$ $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$
$ V_{GS1-2} $ max.	OFFSET VOLTAGE	5	mV	$V_{DG}=10\text{V}$ , $I_D=200\mu\text{A}$

### ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

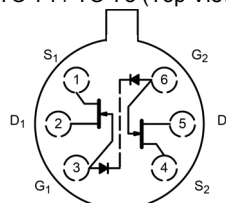
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$BV_{GSS}$	Breakdown Voltage	50	60	--	V	$V_{DS} = 0$ $I_D=1\text{nA}$
$BV_{GGO}$	Gate-To-Gate Breakdown	$\pm 50$	--	--	V	$I_G = 1\text{nA}$ $I_D = 0$ $I_S = 0$
<b>TRANSCONDUCTANCE</b>						
$Y_{fSS}$	Full Conduction	2000	--	7000	$\mu\text{mho}$	$V_{DG} = 10\text{V}$ $V_{GS} = 0\text{V}$ $f = 1\text{kHz}$
$Y_{fS}$	Typical Operation	1000	--	2000	$\mu\text{mho}$	$V_{DG} = 15\text{V}$ $I_D = 200\mu\text{A}$ $f = 1\text{kHz}$
$ Y_{fS1-2}/Y_{fS} $	Mismatch	--	0.6	3	%	
<b>DRAIN CURRENT</b>						
$I_{DSS}$	Full Conduction	0.5	--	10	mA	$V_{DG} = 10\text{V}$ $V_{GS} = 0\text{V}$
$ I_{DSS1-2}/I_{DSS} $	Mismatch at Full Conduction	--	1	5	%	
<b>GATE VOLTAGE</b>						
$V_{GS}(\text{off})$ or $V_p$	Pinchoff voltage	-0.5	--	-2.5	V	$V_{DS} = 15\text{V}$ $I_D = 1\text{nA}$
$V_{GS}(\text{on})$	Operating Range	--	--	-2.3	V	$V_{DS} = 15\text{V}$ $I_D = 200\mu\text{A}$
<b>GATE CURRENT</b>						
$-I_{G\text{max}}$	Operating	--	-4	-15	$\mu\text{A}$	$V_{DG} = 15\text{V}$ $I_D = 200\mu\text{A}$
$-I_{G\text{max}}$	High Temperature	--	--	-10	nA	$T_A = +125^\circ\text{C}$
$-I_{GSS\text{max}}$	At Full Conduction	--	--	100	$\mu\text{A}$	$V_{DS} = 0$
$-I_{GSS\text{max}}$	High Temperature	5	5	5	$\mu\text{A}$	$V_{DG} = 15\text{V}$ $T_A = +125^\circ\text{C}$
<b>OUTPUT CONDUCTANCE</b>						
$Y_{OSS}$	Full Conduction	--	--	20	$\mu\text{mho}$	$V_{DG} = 10\text{V}$ $V_{GS} = 0\text{V}$
$Y_{OS}$	Operating	--	0.2	2	$\mu\text{mho}$	$V_{DG} = 15\text{V}$ $I_D = 500\mu\text{A}$
<b>COMMON MODE REJECTION</b>						
CMR	$-20 \log  V_{GS1-2}/V_{DS} $	95	--	--	dB	$V_{DS} = 10$ to $20\text{V}$ $I_D = 30\mu\text{A}$
<b>NOISE</b>						
NF	Figure	--	--	0.5	dB	$V_{DS} = 15\text{V}$ $V_{GS} = 0\text{V}$ $R_G = 10\text{M}$ $f = 100\text{Hz}$ $\text{NBW} = 6\text{Hz}$
$e_n$	Voltage	--	20	--	nV/Hz	$V_{DS} = 15\text{V}$ $I_D = 200\mu\text{A}$ $f = 10\text{Hz}$ $\text{NBW} = 1\text{Hz}$
<b>CAPACITANCE</b>						
$C_{ISS}$	Input	--	--	8	pF	$V_{DS} = 15\text{V}$ $I_D = 200\mu\text{A}$ $f = 1\text{MHz}$
$C_{RSS}$	Reverse Transfer	--	--	1.5	pF	

### Available Packages:

U401/ LSU401 in TO-71 & TO-78  
U401/ LSU401 in PDIP & SOIC  
U401/ LSU401 available as bare die

Please contact Micross for full package and die dimensions

TO-71 / TO-78 (Top View)



P-DIP / SOIC (Top View)

