

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device types 02, 03, and 04. Made changes to tables I and II.	93-04-15	K. Cottongim
B	Added device type 05. Added case outline Y. Redrew entire document.	96-04-22	K. A. Cottongim
C	Changes in accordance with NOR 5962-R154-96.	96-06-24	Kendall A. Cottongim
D	Update drawing to the current requirements of MIL-PRF-38534.	05-08-17	Raymond Monnin

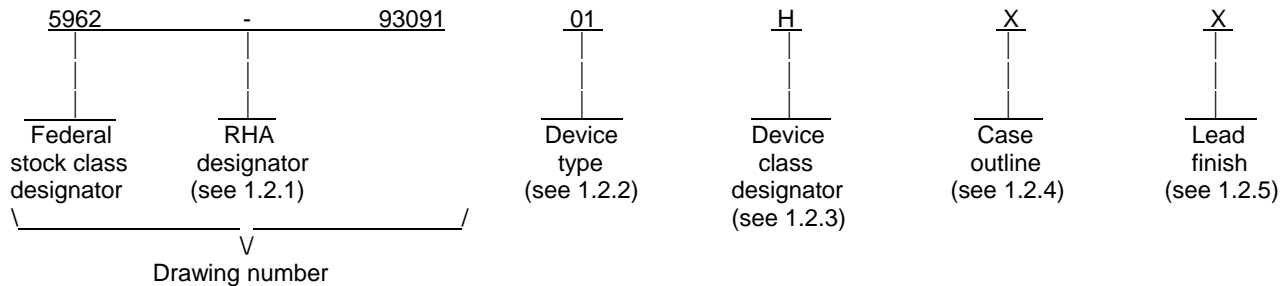
REV																				
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REV	D	D	D	D																
SHEET	15	16	17	18																
REV STATUS OF SHEETS				REV SHEET	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
					1	2	3	4	5	6	7	8	9	10	11	12	13	14	14	

PMIC N/A <p style="text-align: center;">STANDARD MICROCIRCUIT DRAWING</p> <p style="text-align: center;">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p style="text-align: center;">AMSC N/A</p>	PREPARED BY Steve L. Duncan CHECKED BY Michael Jones APPROVED BY Kendall A. Cottongim DRAWING APPROVAL DATE 93-01-22 REVISION LEVEL D	<p>DEFENSE SUPPLY CENTER COLUMBUS POST OFFICE BOX 3990 COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil</p> <p>MICROCIRCUIT, HYBRID, MEMORY, 512K X 8-BIT, ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY</p> <table style="width: 100%; border: none;"> <tr> <td style="border: none;">SIZE A</td> <td style="border: none;">CAGE CODE 67268</td> <td style="border: none;">5962-93091</td> </tr> <tr> <td colspan="3" style="border: none;">SHEET 1 OF 18</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-93091	SHEET 1 OF 18		
SIZE A	CAGE CODE 67268	5962-93091						
SHEET 1 OF 18								

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Access time</u>
01	WE-512K8-150CQ, AS8E512K8CW-150/HQ	EEPROM, 512K x 8-bit	150 ns
02	WE-512K8-300CQ, AS8E512K8CW-300/HQ	EEPROM, 512K x 8-bit	300 ns
03	WE-512K8-250CQ, AS8E512K8CW-250/HQ	EEPROM, 512K x 8-bit	250 ns
04	WE-512K8-200CQ, AS8E512K8CW-200/HQ	EEPROM, 512K x 8-bit	200 ns
05	WE-512K8-200CQ	EEPROM, 512K x 8-bit	200 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

<u>Device class</u>	<u>Device performance documentation</u>
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C, and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 2

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	32	Dual-in-line, dual cavity
Y	See figure 1	32	Dual-in-line, single cavity

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. ^{1/}

Supply voltage range	-0.6 V dc to +6.25 V dc
Input voltage range	-0.6 V dc to +6.25 V dc
Power dissipation (P _D)	1.6 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds).....	+300°C
Thermal resistance, junction-to-case (θ _{JC}).....	28°C/W
Data retention	10 years minimum
Endurance	10,000 cycles minimum

1.4 Recommended operating conditions.

Supply voltage range.....	+4.5 V dc to +5.5 V dc
Input low voltage range (V _{IL}).....	-0.3 V dc to +0.8 V dc
Input high voltage range (V _{IH}).....	+2.2 V dc to V _{CC} + 0.3 V dc
Output voltage, high minimum (V _{OH})	+2.4 V dc
Output voltage, low maximum (V _{OL})	+0.45 V dc
Case operating temperature range (T _C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

^{1/} Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 3

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4, 5, 6, 7, and 8.

3.2.5 Block diagram. The block diagram shall be as specified on figure 9.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Programming procedure. The programming procedure shall be as specified by the manufacturer and shall be available upon request.

3.10 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for the initial characterization and after any design process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 4

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V dc +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC PARAMETERS							
Supply current	I _{CC}	$\overline{CS} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH},$ I/O 0 through I/O 7 = open, inputs = V _{CC} = 5.5 V dc, A0 through A18 change at 5 MHz	1,2,3	All		180	mA
Standby current	I _{SB}	$\overline{CS} = V_{CC},$ I/O 0 through I/O 7 = open, inputs = V _{CC} = 5.5 V dc, A0 through A18 change at 5 MHz	1,2,3	All		10	mA
Input leakage current	I _{LI}	V _{IN} = V _{SS} to V _{CC}	1,2,3	All		80	μA
Output leakage current	I _{LO}	V _{OUT} = V _{SS} to V _{CC}, $\overline{CS} = V_{IH}$}	1,2,3	All		80	μA
Input low voltage	V _{IL}		1,2,3	All		0.8	V
Input high voltage	V _{IH}		1,2,3	All	2.0		V
Output low voltage	V _{OL}	I _{OL} = 2.1 mA, V _{CC} = +4.5 V	1,2,3	All		0.45	V
Output high voltage	V _{OH}	I _{OH} = -400 μA, V _{CC} = +4.5 V	1,2,3	All	2.4		V
FUNCTIONAL TESTING							
Functional tests		See 4.3.1c	7,8A,8B	All			
V _{CC} sense write inhibit	V _{SENS}	See 4.3.1c	7,8A,8B	05	3.0	4.3	V
V _{CC} Power on delay write inhibit	V _{POD}	See 4.3.1c	7,8A,8B	05		10	ms
DYNAMIC CHARACTERISTICS							
Input capacitance	C _{IN}	V _{IN} = 0 V dc <u>2/</u>	4	All		90	pF
Output capacitance	C _{OUT}	V _{OUT} = 0 V dc <u>2/</u>	4	All		120	pF
See footnotes at end of table.							
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990			SIZE A		5962-93091		
					REVISION LEVEL D		SHEET 5

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V dc +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ CYCLE AC TIMING CHARACTERISTICS							
Read cycle time	t _{RC}	See figure 4.	9,10,11	01 02 03 04,05	150 300 250 200		ns
Address access time	t _{ACC}	See figure 4.	9,10,11	01 02 03 04,05		150 300 250 200	ns
Chip select access time	t _{ACS}	See figure 4.	9,10,11	01 02 03 04,05		150 300 250 200	ns
Output hold from address change OE or CS	t _{OH}	See figure 4.	9,10,11	All	0		ns
Output enable to output valid	t _{OE}	See figure 4.	9,10,11	01,04,05 02 03		85 125 100	ns
BYTE WRITE AC TIMING CHARACTERISTICS							
Address setup time	t _{AS}	See figure 5.	9,10,11	All	10		ns
Write pulse width	t _{WP}	See figure 5.	9,10,11	01-04	150		ns
		See figure 5, t _{CS} > 50 ns		05	110		
Chip select setup time	t _{CS}	See figure 5.	9,10,11	All	0		ns
Address hold time	t _{AH}	See figure 5. 3/	9,10,11	All	125		ns
Data valid to end of write	t _{DV}	See figure 5.	9,10,11	All	100		ns
Output enable setup time	t _{OES}	See figure 5.	9,10,11	All	10		ns
Data hold time	t _{DH}	See figure 5.	9,10,11	All	10		ns
Output enable hold time	t _{OEH}	See figure 5.	9,10,11	All	10		ns
See footnotes at end of table.							
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990			SIZE A		5962-93091		
					REVISION LEVEL D		SHEET 6

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V dc +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
BYTE WRITE AC TIMING CHARACTERISTICS - Continued.							
Chip select hold time	t _{CSH}	See figure 5.	9,10,11	All	0 <u>4/</u> 25 <u>5/</u>		ns
Write pulse width high	t _{WPH}	See figure 5.	9,10,11	All	50		ns
PAGE MODE WRITE AC TIMING CHARACTERISTICS							
Data setup time	t _{DS}	See figure 6.	9,10,11	All	100		ns
Data hold time	t _{DH}	See figure 6.	9,10,11	All	10		ns
Write pulse width	t _{WP}	See figure 6.	9,10,11	All	150		ns
Byte load cycle time	t _{BLC}	See figure 6.	9,10,11	All		150	μs
Write pulse width high	t _{WPH}	See figure 6.	9,10,11	All	50		ns
Write cycle time	t _{WC}	See figure 6.	9,10,11	All		10	ms
DATA POLLING AC TIMING CHARACTERISTICS							
Data hold time	t _{DH}	See figure 7.	9,10,11	All	10 <u>4/</u> 35 <u>5/</u>		ns
Output enable hold time	t _{OEH}	See figure 7.	9,10,11	All	10 <u>4/</u> 35 <u>5/</u>		ns
Output enable to output delay	t _{OE}	See figure 7.	9,10,11	All		100	ns
Write recovery time	t _{WR}	See figure 7.	9,10,11	All	0		ns
See footnotes at end of table.							
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990			SIZE A				5962-93091
					REVISION LEVEL D		SHEET 7

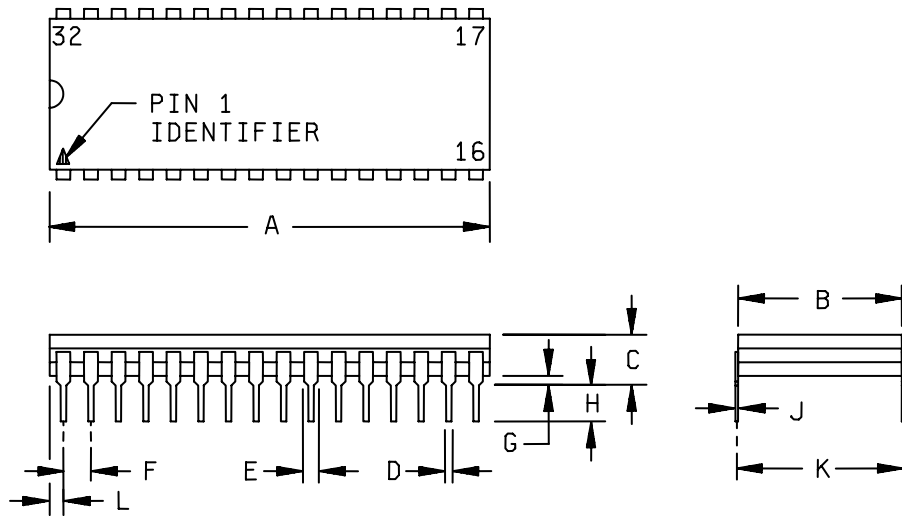
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C V _{SS} = 0 V dc +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CHIP ERASE CHARACTERISTICS							
Setup time <u>6/</u>	t _s	See figure 8.	7,8A,8B	05	5		μs
Pulse width <u>6/</u>	t _w	See figure 8.	7,8A,8B	05	10		ms
Chip erase voltage	V _H		7,8A,8B	05	11.4	12.6	V
Hold time <u>6/</u>	t _H	See figure 8.	7,8A,8B	05	5		μs

- 1/ Unless otherwise specified; the AC test conditions are as follows:
 Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.
 Input rise and fall times: 5 ns.
 Input and output timing reference levels: 1.5 V.
- 2/ Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be guaranteed to the limits specified in table I for all lots not specifically tested.
- 3/ A17 and A18 must remain valid through the WE and CS low pulse.
- 4/ WE controlled.
- 5/ CS controlled.
- 6/ Data FF for all addresses following sequence.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 8

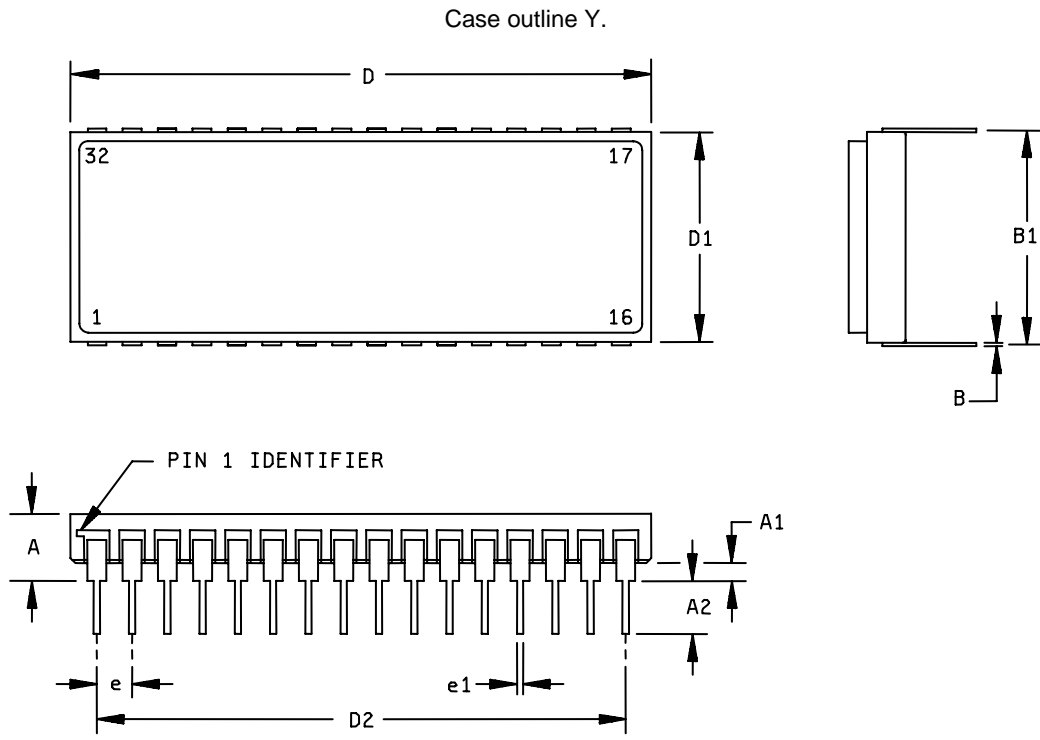
Case outline X.



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	1.654	1.686	42.01	42.82
B	.580	.600	14.73	15.24
C	.235	.275	5.97	6.99
D	.016	.020	0.41	0.51
E	.045	.055	1.14	1.40
F	.100 TYP.		2.54 TYP.	
G	.015	.060	0.38	1.52
H	.125 MIN.		3.18 MIN.	
J	.008	.012	0.20	0.30
K	.590	.610	14.99	15.49
L	.085 TYP.		2.16 TYP.	

FIGURE 1. Case outline(s).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 9



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
D	1.654	1.686	42.01	42.82
D1	.580	.600	14.73	15.24
A	.161	.181	4.10	4.60
e1	.016	.020	0.41	0.51
D2	1.492	1.508	38.02	38.30
e	.100 TYP.		2.54 TYP.	
A1	.027	.047	0.69	1.14
A2	.125 MIN.		3.18 MIN.	
B	.009	.012	0.23	0.30
B1	.590	.610	14.99	15.49

NOTE: The U.S. government preferred system of measurement is the metric SI. These case outlines were designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s) - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 10

Device types	01 - 05
Case outlines	X and Y
Terminal number	Terminal connection
1	A18
2	A16
3	A15
4	A12
5	A7
6	A6
7	A5
8	A4
9	A3
10	A2
11	A1
12	A0
13	I/O 0
14	I/O 1
15	I/O 2
16	V _{SS}
17	I/O 3
18	I/O 4
19	I/O 5
20	I/O 6
21	I/O 7
22	CS
23	A10
24	OE
25	A11
26	A9
27	A8
28	A13
29	A14
30	A17
31	WE
32	V _{CC}

FIGURE 2. Terminal connections.

\overline{CS}	\overline{OE}	\overline{WE}	A0-A18	MODE	DATA I/O	DEVICE CURRENT
H	X	X	X	Standby	High Z	Standby
L	L	H	Stable	Read	Data Out	Active
L	H	L	Stable	Write	Data In	Active
X	H	X	X	Out Disable	High Z	Active
X	X	H	X	Write inhibit	High Z/Data out	Active
X	L	X	X	Write inhibit	High Z/Data out	Active

NOTES:

1. H = V_{IH} = High Logic Level
2. L = V_{IL} = Low Logic Level
3. X = Do not care (either High or Low)
4. High Z = High Impedance state

FIGURE 3. Truth table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 11

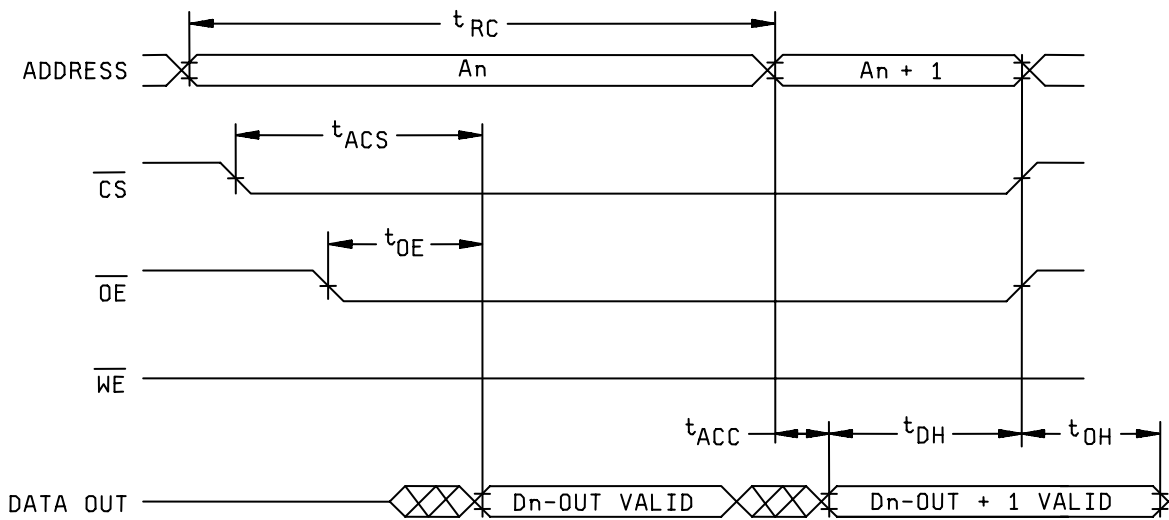
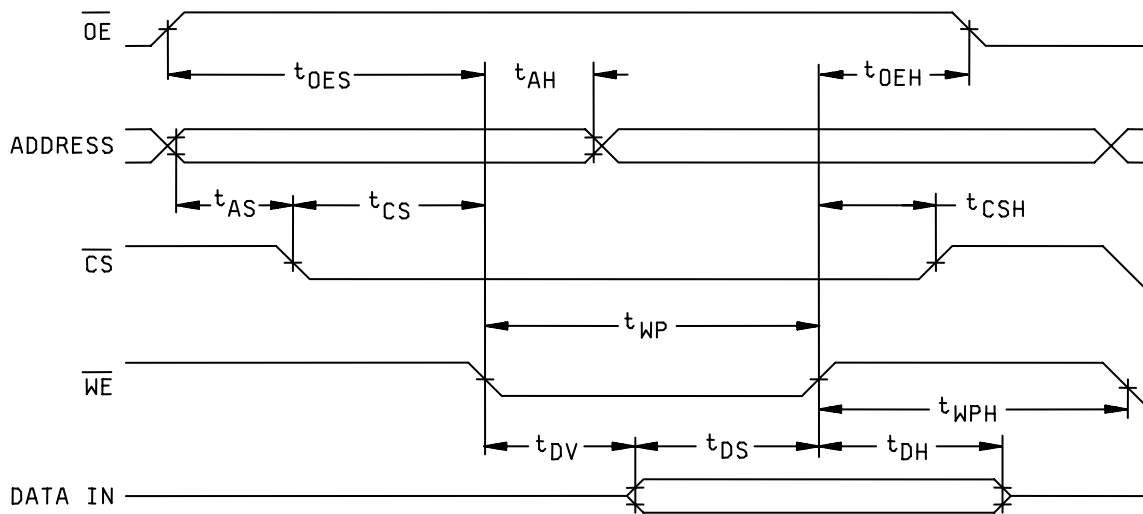


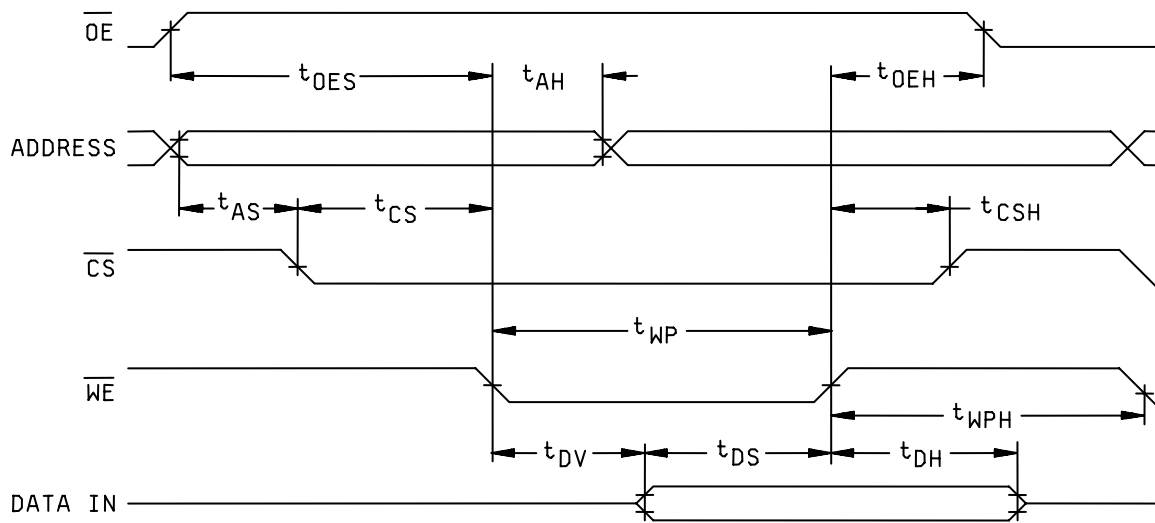
FIGURE 4. Read cycle timing diagram.



\overline{WE} controlled

FIGURE 5. Write cycle timing diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 12



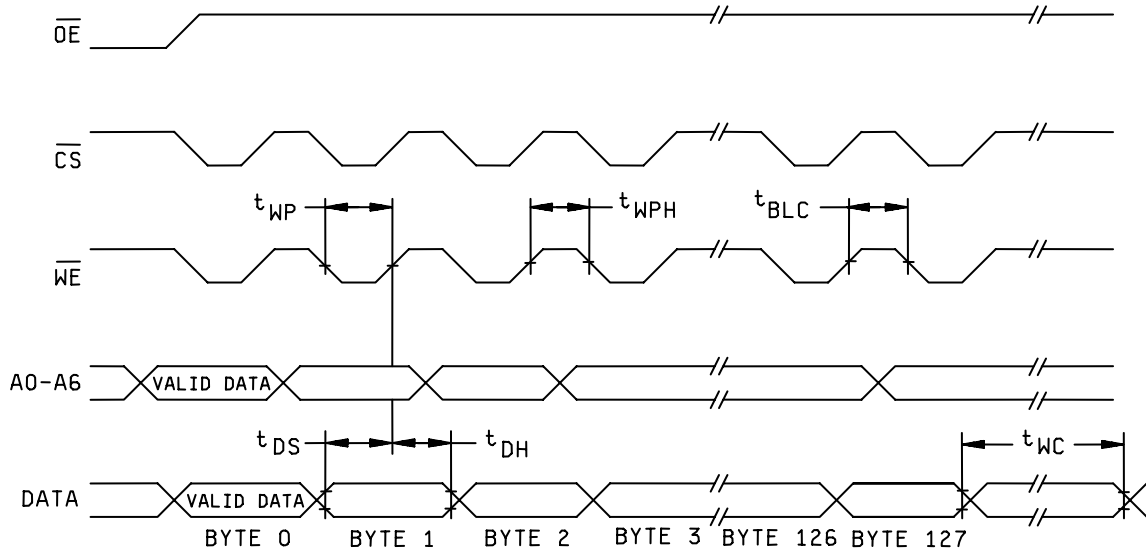
NOTES:

1. A write cycle is initiated when \overline{OE} is high and \overline{WE} or \overline{CS} is pulsed low when \overline{WE} or \overline{CS} is low. The address is latched on the falling edge of \overline{WE} or \overline{CS} , whichever occurs first. In either case, the address setup requirement applies to the falling edge of \overline{CS} due to the inclusion of an address decoder in the device.
2. Due to the inclusion of the address decoder in the device, the \overline{WE} and \overline{CS} write control timings will vary. When utilizing the \overline{CS} controlled write operation, all hold timings must be extended by the 25 ns propagation delay of the address decoder. For \overline{WE} controlled write operation, \overline{CS} must be a minimum of 125 ns to accommodate the additional setup time required.
3. The delay required from the previous write operation to the next must be a minimum of 10 μ s.

\overline{CS} controlled

FIGURE 5. Write cycle timing diagram - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 13



NOTES:

1. A17 and A18 are used to select one of four separate blocks within the device.
2. A7 through A16 are used to specify the page address and must be the same throughout a single page mode write.
3. A0 through A6 are used to address specific bytes within a page.
4. Parameter t_{WC} is the write cycle time which will begin 150 μs after the last byte has been loaded.
5. A write cycle is initiated when \overline{OE} is high and \overline{WE} or \overline{CS} is pulsed low when \overline{CS} or \overline{WE} is low. The address is latched on the falling edge of \overline{WE} or \overline{CS} , whichever occurs last. In either case, the address setup requirement applies to the falling edge of \overline{CS} due to the inclusion of an address decoder in the device, (See figure 5).
6. The delay required from the previous write operation to the next must be a minimum of 10 μs .

FIGURE 6. Page mode write timing diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 14

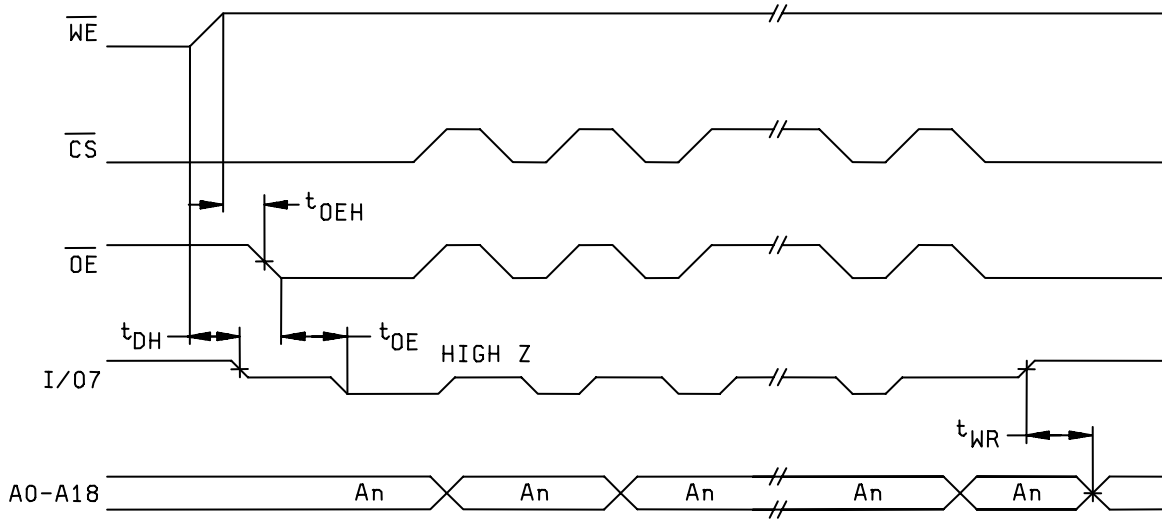


FIGURE 7. Data polling AC timing diagram.

Device type 05 only.

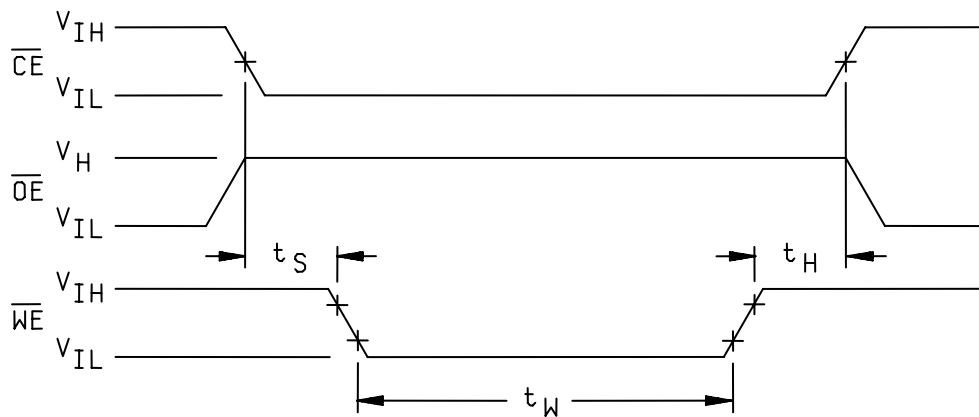


FIGURE 8. Chip erase waveforms.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 15

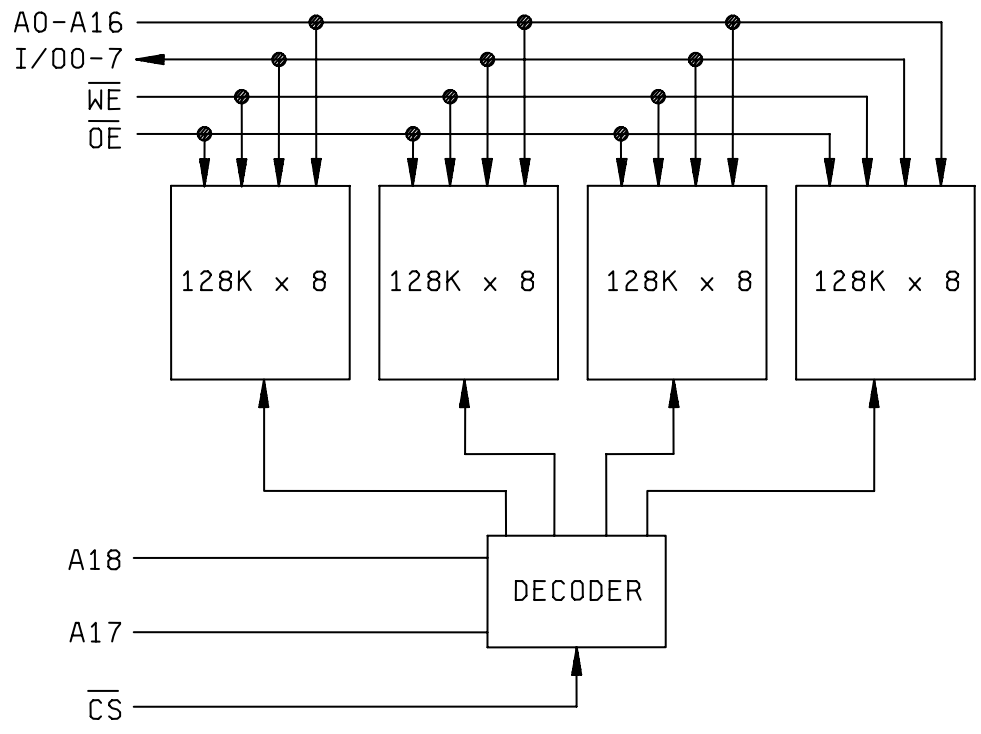


FIGURE 9. Block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 16

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.
 - (3) Prior to burn-in all devices shall be programmed with a 00 hex data pattern to the entire memory array. The resulting pattern shall be verified before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall not be delivered.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 shall be omitted.
- c. Subgroups 7, 8A, and 8B shall include verification of the truth table on figure 3.
- d. The following data patterns shall be verified during subgroups 7, 8A, and 8B:
 - (1) 0's to all memory cell locations.
 - (2) 1's to all memory cell locations.
 - (3) Checkerboard pattern to entire memory array.
 - (4) Checkerboard compliment to entire memory array.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. All devices requiring end-point electrical testing shall be programmed with a checkerboard pattern of alternate rows of AA hex and 55 hex.
- c. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
 - (4) The checkerboard data pattern shall be verified after burn-in as part of end-point electrical testing.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 17

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1, 4, 9
Final electrical parameters	1*, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Group A test requirements	1, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters	1*, 2, 3, 4, 7, 8A, 8B, 9, 10, 11
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Post Office Box 3990, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-93091
		REVISION LEVEL D	SHEET 18

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-08-17

Approved sources of supply for SMD 5962-93091 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9309101HXA 5962-9309101HXC	54230 54230	WE-512K8-150CQ WE-512K8-150CQ
5962-9309101HYA 5962-9309101HYC	54230 54230	WE-512K8-150CQ WE-512K8-150CQ
5962-9309101HYA 5962-9309101HYC	0EU86 0EU86	AS8E512K8CW-150/HQ AS8E512K8CW-150/HQ
5962-9309102HXA 5962-9309102HXC	54230 54230	WE-512K8-300CQ WE-512K8-300CQ
5962-9309102HYA 5962-9309102HYC	54230 54230	WE-512K8-300CQ WE-512K8-300CQ
5962-9309102HYA 5962-9309102HYC	0EU86 0EU86	AS8E512K8CW-300/HQ AS8E512K8CW-300/HQ
5962-9309103HXA 5962-9309103HXC	54230 54230	WE-512K8-250CQ WE-512K8-250CQ
5962-9309103HYA 5962-9309103HYC	54230 54230	WE-512K8-250CQ WE-512K8-250CQ
5962-9309103HYA 5962-9309103HYC	0EU86 0EU86	AS8E512K8CW-250/HQ AS8E512K8CW-250/HQ
5962-9309104HXA <u>3/</u> 5962-9309104HXC <u>3/</u>	54230 54230	WE-512K8-200CQ WE-512K8-200CQ
5962-9309104HYA 5962-9309104HYC	54230 54230	WE-512K8-200CQ WE-512K8-200CQ

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Case outline X for device type 04 is no longer available and not recommended for new design. Case outline Y can be substituted for case outline X.

STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued.

DATE: 05-08-17

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9309104HYA 5962-9309104HYC	0EU86 0EU86	AS8E512K8CW-200/HQ AS8E512K8CW-200/HQ
5962-9309105HYA 5962-9309105HYC	54230 54230	WE-512K8-200CQ WE-512K8-200CQ

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Case outline X for device type 04 is no longer available and not recommended for new design. Case outline Y can be substituted for case outline X.

Vendor CAGE
number

Vendor name
and address

0EU86

Austin Semiconductor Incorporated
8701 Cross Park Drive
Austin, TX 78754-4566

54230

White Electronics Designs Corporation
3601 East University Drive
Phoenix, AZ 85034

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