REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. - CFS	06-01-26	Thomas M. Hess

REV																				
SHEET																				
REV	A	A	A	A	A	A	A													
SHEET	15	16	17	18	19	20	21													

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Christopher A. Rauch

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Tim H. Noh

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
93-02-18

REVISION LEVEL
A

MICROCIRCUIT, DIGITAL, INTERFACE, TRANSPARENT ASYNCHRONOUS TRANSMITTER, MONOLITHIC SILICON

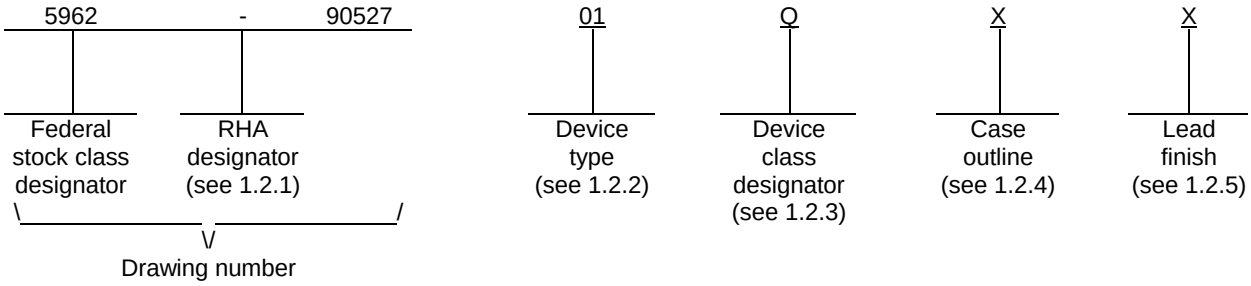
SIZE	CAGE CODE	
A	**67268**	**5962-90527**

SHEET 1 OF 21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7968-125V	Transparent asynchronous transmitter interface

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC2-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) to ground potential continuous	-0.5 V dc to +7.0 V dc
DC voltage range applied to outputs	-0.5 V dc to V_{CC} maximum
DC input voltage range (V_{IN})	-0.5 V dc to + 5.5 V dc
DC output current	±100 mA
DC input current range	-30 mA to +5.0 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	2.1 W 2/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Maximum junction temperature (T_J)	+155°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.75 V dc to +5.5 V dc
Minimum high-level input voltage (V_{IH})	2.1 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added P_D due to short circuit test, e.g., I_{SC}.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Functional block/logic diagram. The functional block/logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 104 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Bus interface signals: DI_0-DI_7, DI_8/CI_3, DI_9/CI_2, CI_0-CI_1, STRB, ACK, CLK							
Output high voltage ACK, CLK	V_{OH}	V_{CC} = 4.75 V, I_{OH} = -1 mA, V_{IN} = 0.0 V or 3.0 V	1, 2, 3	All	2.4		V
Output low voltage ACK, CLK	V_{OL}	V_{CC} = 4.75 V, I_{OL} = 8 mA, V_{IN} = 0.0 V or 3.0 V				0.45	V
Input high voltage	V_{IH}	V_{CC} = 5.5 V 2/			2.1		V
Input low voltage	V_{IL}	V_{CC} = 5.5 V 2/				0.8	V
Input clamp voltage	V_I	V_{CC} = 4.75 V, I_{IN} = -18 mA				-1.5	V
Input low current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V				-400	µA
Input high current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 2.7 V				50	µA
Input leakage current	I_I	V_{CC} = 5.5 V, V_{IN} = 5.5 V; All inputs except CLK				50	µA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V; CLK input				150	
Output short circuit current ACK, CLK	I_{SC}	3/			-15	-85	mA
Serial interface signals: SEROUT+, SEROUT-							
Output high voltage	V_{OH}	V_{CC} = 4.75 V, ECL load	1, 2, 3	All	V_{CC} – 1.165	V_{CC} – 0.88	V
Output low voltage	V_{OL}	V_{CC} = 4.75 V, ECL load			V_{CC} – 1.81	V_{CC} – 1.62	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Miscellaneous signals: X_1, V_{CC1}, V_{CC2}, V_{CC3}							
Input high voltage X_1	V_{IHX}	V_{CC} = 5.5 V 2/	1, 2, 3	All	2.1		V
Input low voltage X_1	V_{ILX}					0.8	V
Input low current X_1	I_{ILX}	V_{IN} = 0.45 V				-900	µA
Input high current X_1	I_{IHX}	V_{IN} = 2.4 V				+600	µA
Supply current	I_{CC}	SEROUT = ECL load, DMS = 0, $V_{CC1} = V_{CC2} = V_{CC3}$ = 5.5 V; pin V_{CC1} (TTL)				30	mA
		pin V_{CC2} (ECL)				45	
		pin V_{CC3} (CML)				215	
Bus interface signals: DI_0-DI_7, DI_8/CI_3, DI_9/CI_2, CI_0-CI_1, STRB, ACK, CLK							
CLK period	t_1	See figure 4. 4/	9, 10, 11	All	8n	25n	ns
CLK pulse width high	t_2				25		ns
CLK pulse width low	t_3				25		ns
STRB pulse width high 5/	t_4				20		ns
STRB pulse width low	t_5				20		ns
Internal byte boundary to CLK↓ 6/	t_6				$(-9t_1/8n) + 3$	25	ns
Data-STRB setup time	t_9				10		ns
Data-STRB hold time	t_{10}				15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Bus interface signals: DI_0-DI_7, DI_8/CI_3, DI_9/CI_2, CI_0-CI_1, STRB, ACK, CLK - Continued.							
ACK ↑ to STRB ↓ hold 7/	t_{11}	See figure 4. 4/ TTL output load	9, 10, 11	All	0		ns
ACK ↓ to STRB ↑ hold	t_{12}				0		ns
STRB ↑ to ACK ↑ 8/	t_{13}					45	ns
STRB ↓ to ACK ↓	t_{14}					25	ns
CLK ↓ to ACK ↑ 8/	t_{15}					$(3t_1/n) + 43$	ns
Miscellaneous signals: X_1 9/							
X_1 pulse width high 10/	t_{29}	See figure 4. TTL output load on CLK	9, 10, 11	All	35		ns
X_1 pulse width low 10/	t_{30}				35		ns
X_1 ↑ to CLK ↑	t_{32}	See figure 4. TTL load				32	ns
X_1 ↓ to CLK ↓	t_{33}					32	ns

1/ Unless otherwise specified, for dc test parameters, all test conditions shall be worst case conditions; V_{IH} = 2.1 V and V_{IL} = 0.8 V. For ac test parameters, all tests are performed using the input waveforms shown in figure 4.

The following conditions also apply:

All timing references are made with respect to +1.5 V for TTL-level signals or to the 50 percent point between V_{OH} and V_{OL} for ECL signals. ECL input rise and fall times must be 2 ns ±0.2 ns between 20 percent and 80 percent points. TTL input rise and fall times must be 2 ns ±0.2 ns between 1 V and 2 V.

2/ Measured with device in test mode while monitoring output logic states.

3/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4/ Switching characteristics are tested during 8 bit local mode operation.
"Data" is DI_0 - DI_7 or DI_8/CI_3 or DI_9/CI_2 or CI_0 - CI_1.
"n" is determined by the following:

DMS	TLS	"n"
GND	Open	8 bit n = 1; Test mode 2
	GND/V_{CC}	8 bit n = 10; Local/Test mode 1
V_{CC}	Open	9 bit n = 1; Test mode 2
	GND/V_{CC}	9 bit n = 11; Local/Test mode 1
Open or 1/2 V_{CC}	Open	10 bit n = 1; Test mode 2
	GND/V_{CC}	10 bit n = 12; Local/Test mode 1

5/ t_4 guarantees that data is latched. ACK (t_{11}) timing may not be valid.

6/ t_6 (Internal Byte Boundary to CLK ↓) is created by the variation of internal STRB propagation delays relative to internal byte boundaries over temperatures and V_{CC}. The internal byte boundary determines the byte in which data will come out (at SEROUT±). If STRB occurs before the byte boundary, then the data will be sent out two bytes later. If STRB occurs after the byte boundary, then the output data will be delayed by one additional byte.

7/ If t_{11} is not met, ACK response and timing are not guaranteed, but data will still be latched on STRB ↑ (see t_4).

8/ ACK delay is determined by t_{13} when the input latch is empty or by t_{15} when the latch is full (Busy mode). Also note that ACK will not rise if STRB does not remain HIGH until ACK rises.

9/ Jitter on X_1 input must be less than ±0.2 ns, to ensure that automatic test equipment can properly measure device switching characteristics.

10/ X_1 Pulse Width is measured at a point where CLK output exactly meets CLK (t_2 or t_3) specification limit.

Cases X and 3

Pin or terminal number	Symbol	Pin or terminal number	Symbol
1	ACK	15	DI_8/CI_3
2	STRB	16	DI_7
3	SEROUT+	17	DI_6
4	SEROUT-	18	CLK
5	V_{CC2} (ECL)	19	X_2
6	V_{CC1} (TTL)	20	X_1
7	V_{CC3} (CML)	21	GND_2 (CML)
8	RESET	22	GND_1 (TTL)
9	DMS	23	DI_0
10	TLS	24	DI_1
11	TSERIN	25	DI_2
12	CI_0	26	DI_3
13	CI_1	27	DI_4
14	DI_9/CI_2	28	DI_5

FIGURE 1. Terminal connections.

Encoder patterns					
4B/5B encoder scheme			5B/6B encoder scheme		
Hex data	4-bit binary data	5-bit encoded symbol	Hex data	5-bit binary data	6-bit encoded symbol
0	0000	11110	00	00000	110110
1	0001	01001	01	00001	010001
2	0010	10100	02	00010	100100
3	0011	10101	03	00011	100101
4	0100	01010	04	00100	010010
5	0101	01011	05	00101	010011
6	0110	01110	06	00110	010110
7	0111	01111	07	00111	010111
8	1000	10010	08	01000	100010
9	1001	10011	09	01001	110001
A	1010	10110	0A	01010	110111
B	1011	10111	0B	01011	100111
C	1100	11010	0C	01100	110010
D	1101	11011	0D	01101	110011
E	1110	11100	0E	01110	110100
F	1111	11101	0F	01111	110101
			10	10000	111110
			11	10001	011001
			12	10010	101001
			13	10011	101101
			14	10100	011010
			15	10101	011011
			16	10110	011110
			17	10111	011111
			18	11000	101010
			19	11001	101011
			1A	11010	101110
			1B	11011	101111
			1C	11100	111010
			1D	11101	111011
			1E	11110	111100
			1F	11111	111101

NOTE: Hex data is parallel input data which is represented by the 4-bit or 5-bit binary data listed in the column to the immediate right of hex data. Binary bits are listed from left to right in the following order:

8-bit mode = D_7, D_6, D_5, D_4, (4-bit binary), and D_3, D_2, D_1, D_0, (4-bit binary)
9-bit mode = D_8, D_7, D_6, D_5, D_4, (5-bit binary), and D_3, D_2, D_1, D_0, (4-bit binary)
10-bit mode = D_8, D_7, D_6, D_5, D_4, (5-bit binary), and D_9, D_3, D_2, D_1, D_0, (5-bit binary)

Serial bits are shifted out with the most significant bit of the most significant nibble coming out first.

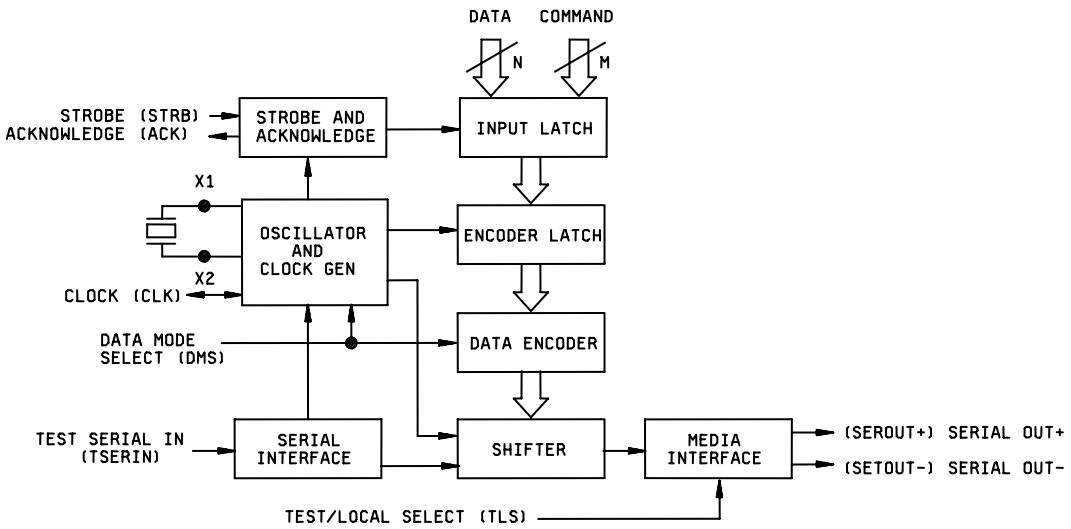
FIGURE 2. Truth tables.

Command symbols					
Transparent Asynchronous Transmitter (5962-90527)				Transparent Asynchronous Receiver (5962-90528)	
Command input				Command output	
Hex	Binary	Encoded symbol	Mnemonic	Hex	Binary
Symbol 8-bit transparent asynchronous transmitter interface					
0	0000	XXXXX XXXXX	Data	No change (see note 2)	No change (see note 2)
No STRB (see note 1)	No STRB (see note 1)	11000 10001	JK (8-bit sync)	0	0000
1	0001	11111 11111	II	1	0001
2	0010	01101 01101	TT	2	0010
3	0011	01101 11001	TS	3	0011
4	0100	11111 00100	IH	4	0100
5	0101	01101 00111	TR	5	0101
6	0110	11001 00111	SR	6	0110
7	0111	11001 11001	SS	7	0111
8 (see note 3)	1000	00100 00100	HH	8	1000
9	1001	00100 11111	HI	9	1001
A (see note 3)	1010	00100 00000	HQ	A	1010
B	1011	00111 00111	RR	B	1011
C	1100	00111 11001	RS	C	1100
D (see note 3)	1101	00000 00100	QH	D	1101
E (see note 3)	1110	00000 11111	QI	E	1110
F (see note 3)	1111	00000 00000	QQ	F	1111
9-bit transparent asynchronous transmitter interface					
0	000	XXXXXX XXXXX	Data	No change (see note 2)	No change (see note 2)
No STRB (see note 1)	No STRB (see note 1)	011000 100011	LK (9-bit sync)	0	000
1	001	111111 11111	I'I	1	001
2	010	011101 01101	T'T	2	010
3	011	011101 11001	T'S	3	011
4	100	111111 00100	I'H	4	100
5	101	011101 00111	T'R	5	101
6	110	111001 00111	S'R	6	110
7	111	111001 11001	S'S	7	111
10-bit transparent asynchronous transmitter interface					
0	00	XXXXXX XXXXXX	Data	No change (see note 2)	No change (see note 2)
No STRB (see note 1)	No STRB (see note 1)	011000 100011	LM (10-bit sync)	0	00
1	01	111111 111111	I'I'	1	01
2	10	011101 011101	T'T'	2	10
3	11	011101 111001	T'S'	3	11

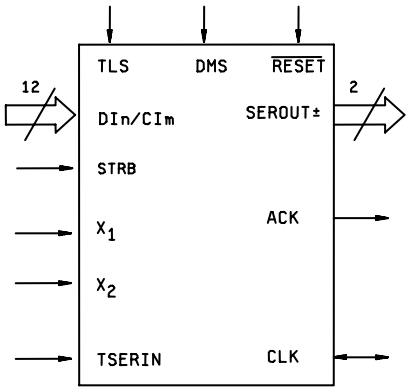
NOTES:
1. Command pattern sync cannot be explicitly sent by the transmitter with any combination of inputs and STRB, but is used to pad between user data.
2. A strobe with all 0's on the command input lines will cause data to be sent. See figure 2 (encoder patterns).
3. While these commands are legal data and will not disrupt normal operation if used occasionally, they may cause data errors if grouped into recurrent fields. Normal PLL operation cannot be guaranteed if one or more of these commands is continuously repeated.

FIGURE 2. Truth tables - Continued.

Functional block diagram



Logic symbol



NOTE: N can be 8, 9, or 10 bits total of N + M = 12.

FIGURE 3. Functional block/logic diagram.

Key to switching waveforms

WAVEFORM SYMBOL	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

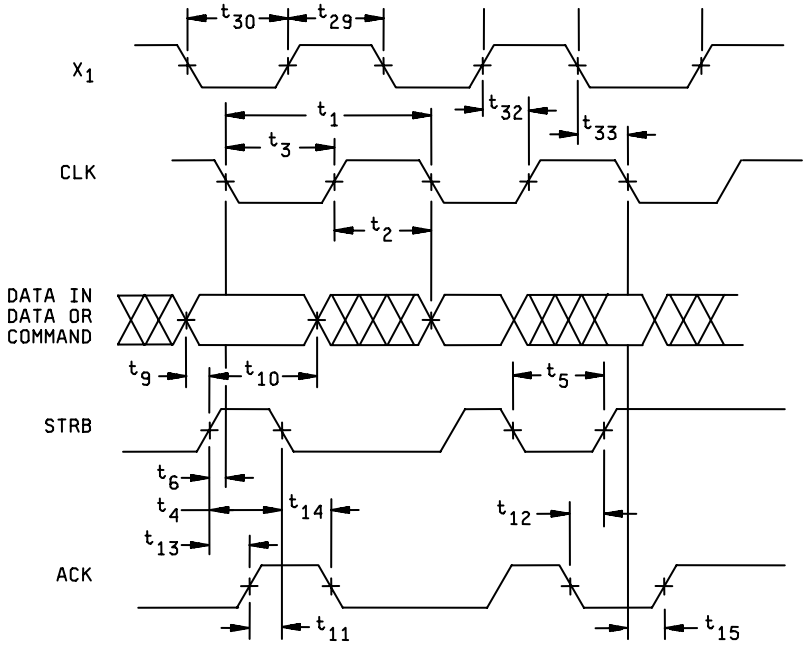
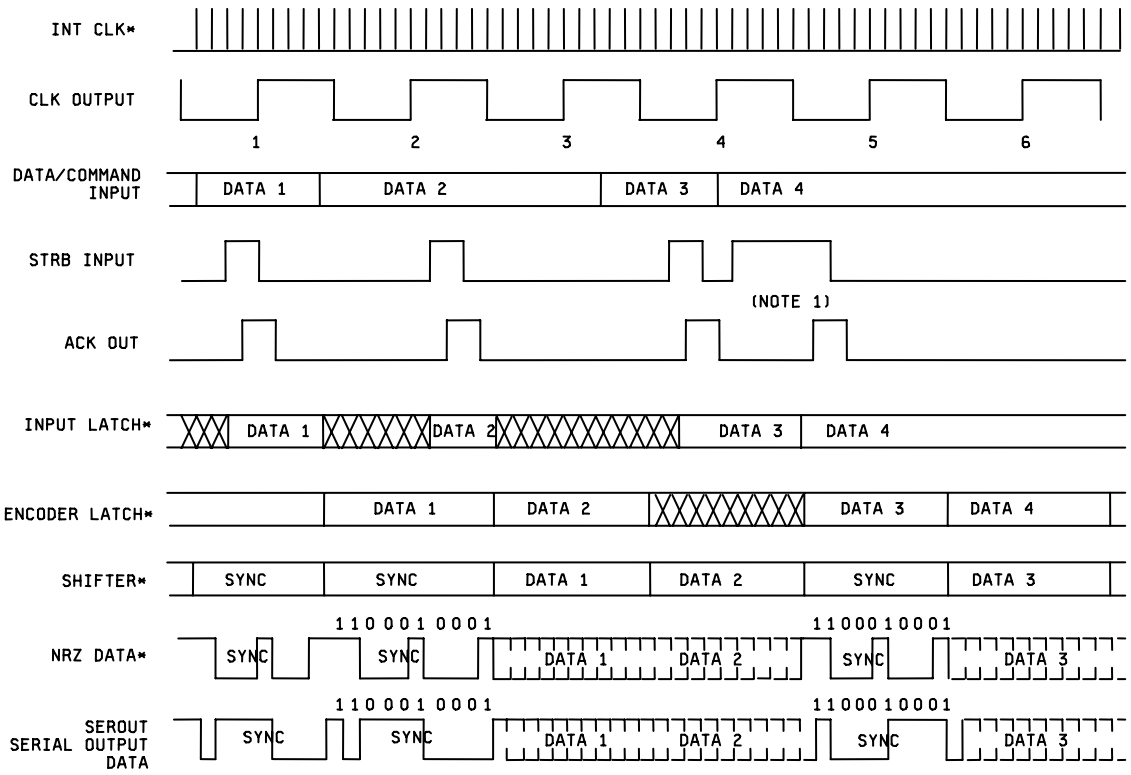


FIGURE 4. Switching waveforms and test circuit.

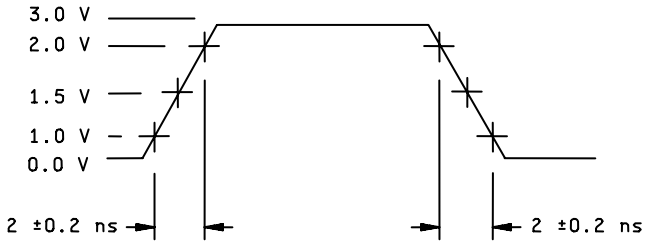


NOTES:

* = Internal signals.

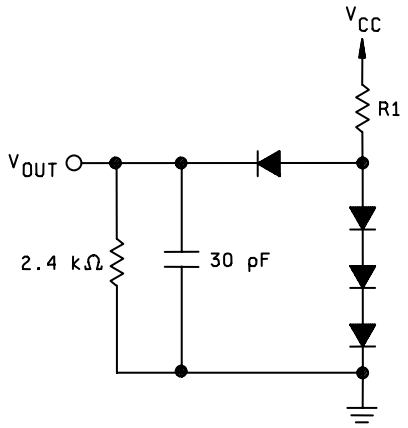
1. The input latch is BUSY when the second STRB comes in; the internal STR-ACK is delayed until the next CLK window

FIGURE 4. Switching waveforms and test circuit - Continued.



TTL INPUT WAVEFORM

(USED FOR TABLE I
AC ELECTRICAL
PERFORMANCE TESTING)

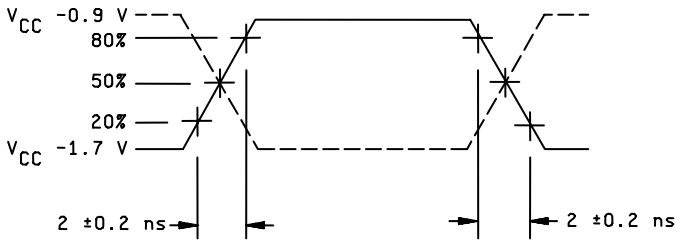


TTL OUTPUT LOAD

NOTES:

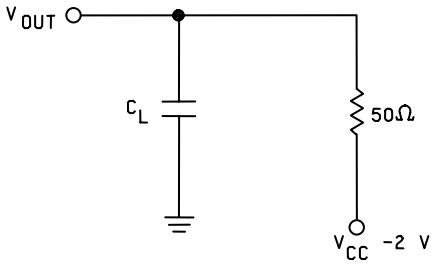
1. R_1 = 500Ω for the I_{OL} = 8 mA.
2. All diodes 1N916 or 1N3064, or equivalent.
3. $C_L \leq 30$ pF includes scope probe, wiring, and stray capacitance without device in test fixture.
4. Automatic test equipment load configurations and forcing functions are used, therefore this load figure is for reference only.

FIGURE 4. Switching waveforms and test circuit - Continued.



ECL INPUT WAVEFORM

(USED FOR TABLE I
AC ELECTRICAL
PERFORMANCE TESTING)



ECL OUTPUT LOAD

NOTES:
1. $C_L \leq 3$ pF includes scope probe, wiring, and stray capacitance without device in test fixture.
2. Automatic test equipment load configurations and forcing functions are used, therefore this load figure is for reference only.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1, 7
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and in table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Pin description.

Symbol	Name and function
$DI_0 – DI_7$	Parallel data in (TTL inputs). These eight inputs accept parallel data from the host system, to be latched, encoded and transmitted.
DI_8/CI_3	Parallel data (8) in or command (3) in (TTL input). DI_8/CI_3 input is either data or command, depending upon the state of DMS.
DI_9/CI_2	Parallel data (9) in or command (2) in (TTL input). DI_9/CI_2 input is either data or command, depending upon the state of DMS.
$CI_0 – CI_1$	Parallel command in (TTL inputs). These two inputs accept parallel command information and host system. If one or more command bits are logic "1", the command bit pattern is latched, encoded, and transmitted in place of any pattern on the Data inputs.
STRB	Input strobe signal (TTL input). A rising edge on the STRB input causes the Data (DI_0-DI_9) or the command (CI_0-CI_3) inputs to be latched into the transmitter. The STRB signal is normally taken LOW, after ACK has risen.
ACK	Input-strobe acknowledge (TTL output). The rising edge of ACK signifies that the transmitter is ready to accept new data and command. The timing of ACK's response to STRB depends on the condition of the input latch (in a given CLK cycle). If the input latch is empty, data is immediately stored and ACK closely follows STRB. If the input latch contains previously stored data when STRB is asserted, ACK is delayed until the next falling edge of CLK. Note that for ACK to rise STRB must remain HIGH for both of the above conditions.
SEROUT+, SEROUT-	Differential serial data out (differential open emitter ECL outputs). These differential ECL outputs generate data at ECL voltage levels referenced to +5.0 V. When connected to appropriate pull down resistors, they are capable of driving 50 ohm terminated lines, either directly or through isolating capacitors.
X_1, X_2	Crystal 1 (input), crystal 2 (output). These two crystal pins connect to an internal parallel mode oscillator which operates at the fundamental frequency of the crystal. The byte rate matches the crystal frequency. Alternatively, X_1 can be driven by an external TTL frequency source. In multiple device systems this external source could be another devices CLK output. In this case, crystal 2 should be left open.
DMS	Data mode select (input). Data mode select input determines the data pattern width. When it is wired to GND, the device transmitter will assume data to be eight bits wide, with four bits of command. When it is wired to V_{CC}, the device transmitter will assume data to be nine bits wide, with three bits of command. If DMS is left floating (or terminated to 1/2 V_{CC}), the device will assume data to be ten bits wide, with two bits of command.

TABLE III. Pin description - Continued.

Symbol	Name and function
TLS	Test/local select (input). TLS input determines the mode of operation. When TLS is wired to GND, the device transmitter assumes a local mode connection to the media. It will output NRZI encoded data, and will enable its CLK output driver. TLS pin should always be grounded during local mode operation. When this input is left unconnected, it floats to an intermediate level which puts the device transmitter into its test mode 2. In test mode 2, the internal clock multiplier is switched out, and the internal logic is clocked directly from the CLK pin. Test mode 2 is included to ease automatic test equipment (A.T.E.) testing by making the internal logic of the device synchronous to the external clock instead of the internal PLL. When TLS is wired to V_{CC} (test mode 1), the device performs an internal factory test function.
CLK	Clock (TTL I/O). CLK is an I/O pin that supplies the byte-rate clock reference to drive all internal logic. When TLS is connected to ground (local mode), CLK is enabled as a free-running (byte-rate) clock output which runs at the crystal oscillator frequency; this output can be used to drive the X_1 input of the devices receivers or other system logic. In test mode CLK becomes an input. In test mode 1, CLK is a byte rate input and in test mode 2, it is a bit rate input.
$\overline{\text{RESET}}$	PLL RESET (input). This pin is normally left open, but can be momentarily (1 ms minimum) grounded to force the internal PLL to reactivate lock. This allows for correction in the unlikely occurrence of PLL lockup on application of power. RESET has an internal pull-up resistor which causes it to float high when left unconnected (50 KΩ nominal).
TSERIN	Test serial input (pseudo ECL input). This pin performs an internal factory test function. During local mode and test mode 2 operation, this pin should be left open.
V_{CC1}, V_{CC2}, V_{CC3}	Power supply. V_{CC1}, V_{CC2} and V_{CC3} are +5.0 volt nominal power supply pins. V_{CC1} powers TTL, V_{CC2} powers ECL, and V_{CC3} powers logic and analog circuitry.
GND_1, GND_2	Ground pins. GND_1 is a TTL ground and GND_2 is logic and analog ground.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-01-26

Approved sources of supply for SMD 5962-90527 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9052701MXA	3/	AM7968-125V/BXA
5962-9052701M3A	0EU86	AS7968EC28
5962-9052701QXA	0EU86	AS7968C28

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor, Inc. 8701 Cross Park Drive Austin, TX 78764