REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Boilerplate update, part of 5 year review. ksr	06-10-31	Raymond Monnin

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	A	A	A	A																
SHEET	15	16	17	18																

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
89-12-12

REVISION LEVEL
A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 16K X 4 STATIC RAM (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89692**

SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89692	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Acess time
01		16K X 4 static ram	25 ns (data retention)
02		"	25 ns
03		"	20 ns (data retention)
04		"	20 ns
05		"	15 ns (data retention)
06		"	15 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	flat package
X	See figure 1	22	dual-in-line package
Y	See figure 1	22	dual-in-line package
Z	See figure 1	22	leadless chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc 2/
DC output current	20 mA
Ambient storage temperature	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Thermal resistance, junction-to-case (Θ_{JC}):.	
Cases K	See MIL-STD-1835
Case X and Y	28°C/W
Case Z	22°C/W
Power dissipation, (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc 2/
Ground voltage (V_{SS})	0 V dc
Input high voltage (V_{IH})	+2.2 V dc to V_{CC} + 0.5 V dc
Input low voltage (V_{IL})	-0.5 V dc to 0.8 V dc 3/
Operating case temperature range (T_C)	-55°C to +125°C

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.
2/ All voltages referenced to V_{SS}.
3/ V_{IL} negative undershoots to a minimum of -2.0 V dc are allowed with a maximum 20 ns pulse width.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{CC} = max, V_{IN} = GND to V_{CC}	1,2,3	All		10	µA
Output leakage current	I_{LO}	V_{CC} = max; V_{OUT} = GND to V_{CC}, $\overline{CE} \ge V_{IH}$, $\overline{WE} \le V_{IL}$	1,2,3	All		10	µA
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1,2,3	All		0.4	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1,2,3	All	2.4		V
Operating supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, outputs open, V_{CC} = max, f = $1/t_{AVAX}$	1,2,3	01, 03		120	mA
				02, 04		130	
				05, 06		150	
Standby power supply current (TTL)	I_{CC2}	$\overline{CE} \ge V_{IH}$, outputs open, V_{CC} = max, f = 0 MHz	1,2,3	01,03, 05		20	mA
				02,04, 06		50	
Standby power supply current (CMOS)	I_{CC3}	V_{CC} +0.2 V $\ge \overline{CE} \ge$ V_{CC} - 0.2 V, outputs open, V_{CC} +0.2 V $\ge V_{IN} \ge V_{CC}$ - 0.2 V or +0.2 V $\ge V_{IN} \ge$ -0.2 V, f = 0 Mhz	1,2,3	01,03, 05		5	mA
				02,04, 06		20	
Data retention current	I_{CC4}	V_{CC} = V_{DR} = 2.0 V	1,2,3	01,03, 05		600	µA
Input capacitance	C_{IN} 1/	V_I = 0 V, f = 1 Mhz, T_A = +25°C, see 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT} 1/	V_O= 0 V, f = 1 Mhz, T_A = +25°C, see 4.3.1c	4	All		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Read cycle time	t_{AVAX}	See figure 4	9, 10 11	01,02	25		ns
				03,04	20		
				05,06	15		
Address cycle time	t_{AVQV}		9, 10, 11	01,02		25	ns
				03,04		20	
				05,06		15	
Chip enable access time	t_{ELQV}		9, 10, 11	01,02		25	ns
				03,04		20	
				05,06		15	
Output hold from address change	t_{AVQX}		9, 10, 11	01-04	3		ns
				05,06	2		
Chip select to output in low Z	t_{ELQX} 1/ 3/		9, 10, 11	01-04	3		ns
				05,06	2		
Chip select to output in high Z	t_{EHQZ} 1/ 3/		9, 10, 11	All		15	ns
Write enable to output in high Z	t_{WLQZ} 1/ 3/		9, 10, 11	01,02		15	ns
				03,04		12	
				05,06		10	
Data valid to end of write	t_{DVWH}		9, 10, 11	01,02	15		ns
				03,04	12		
				05,06	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data hold time	t_{WHDX}	See figure 4	9, 10, 11	All	0		ns
Output active from end of write	t_{WHQV} 1/ 3/		9, 10, 11	All	3		ns
Write cycle time	t_{AVAV}		9, 10, 11	01,02	25		ns
				03,04	20		
				05,06	15		
Chip select to end of write	t_{ELWH}		9, 10, 11	01,02	20		ns
				03,04	17		
				05,06	14		
Address valid to end of write	t_{AVWH}		9, 10, 11	01,02	20		ns
				03,04	17		
				05,06	14		
Address setup time	t_{AVWL}		9, 10, 11	All	0		ns
Write pulse width	t_{WLWH}		9, 10, 11	01,02	20		ns
				03,04	17		
				05,06	14		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write recovery time	t_{EHAX}	See figure 4	9, 10, 11	01-04	5		ns
				05,06	3		

1/ This parameter tested initially and after any design and or process change which could affect this parameter, and is therefore guaranteed to the limits specified in table I.
2/ AC parameter are tested using input rise and fall times of 5 ns and input pulse levels of GND to 3.0 V. Both input and output timing reference levels are 1.5 V, and the output load is shown on figure 5.
3/ Transition is measured ±500 mV from steady-state.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

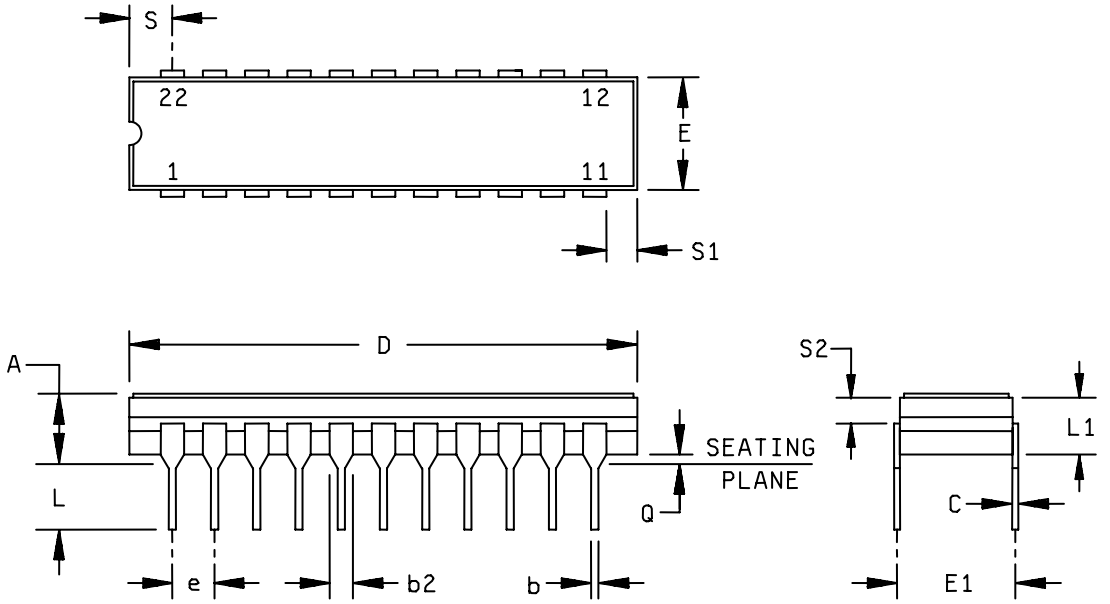
3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Case X



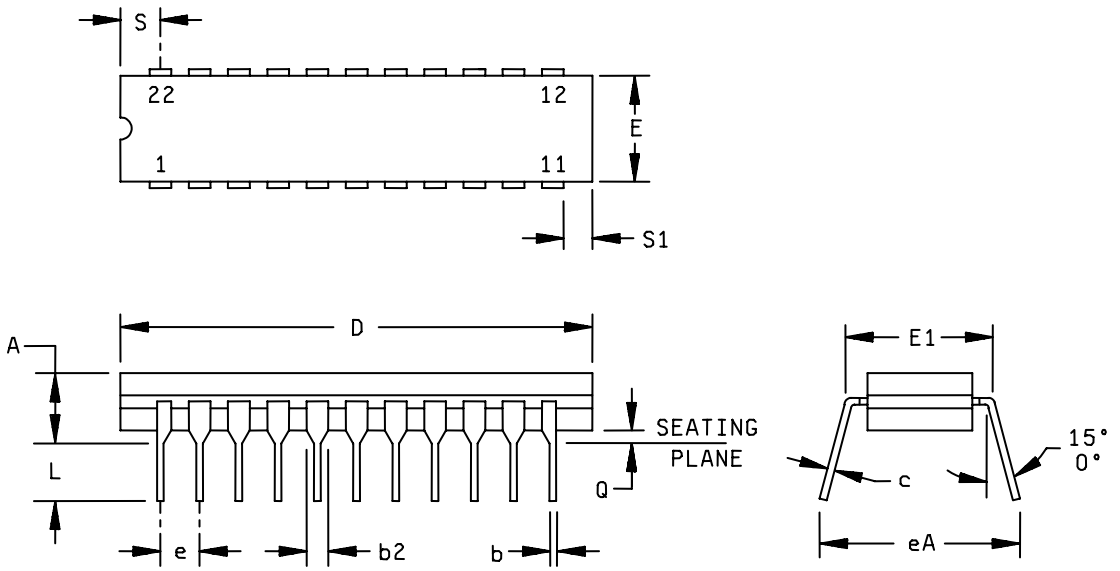
Symbol	Inches	
	Min	Max
A	.100	.200
b	.014	.023
b2	.030	.060
C	.008	.015
D	1.050	1.260
E	.260	.310
E1	.280	.320
e	.100 BSC	
L	.125	.200
L1	.150	
Q	.015	.060
S	.030	.065
S1	.005	
S2	.005	

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

Inches	mm
.005	0.13
.008	0.20
.014	0.36
.015	0.38
.023	0.58
.030	0.76
.060	1.52
.065	1.65
.100	2.54
.125	3.18
.150	3.81
.200	5.08
.260	6.60
.290	7.37
.310	7.87
.320	8.13
1.050	26.67
1.260	32.00

FIGURE 1. Case outlines.

Case Y



Symbol	Inches	
	Min	Max
A	.155	.200
b	.015	.020
b2	.045	.065
C	.009	.012
D	1.060	1.110
E	.245	.310
E1	.290	.320
e	.090	.110
eA	.330	.390
L	.125	.200
Q	.015	.060
S	.025	.045
S1	.005	

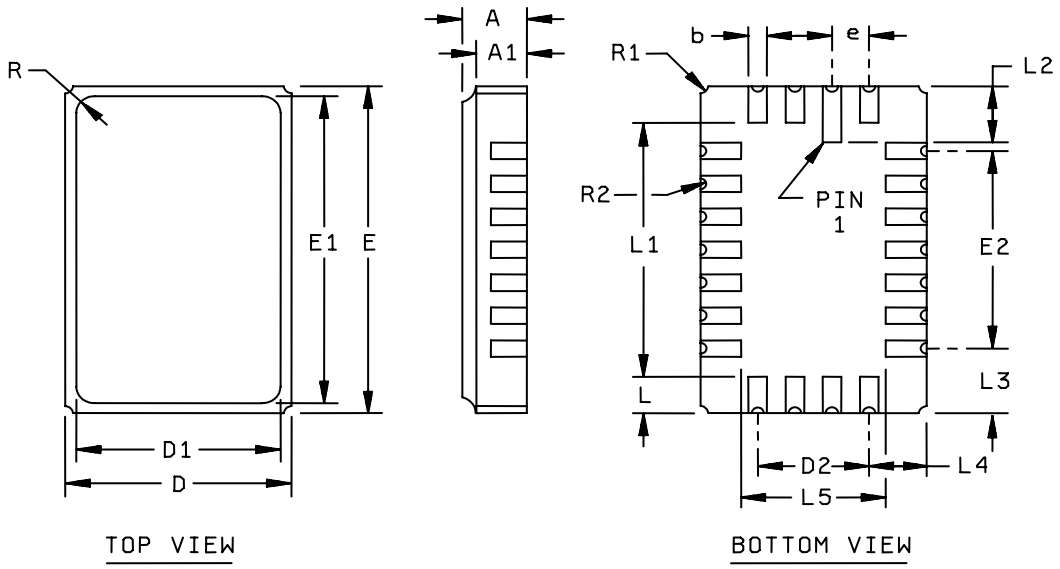
NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

Inches	mm		Inches	mm
.005	0.13		.200	5.08
.009	0.22		.245	6.22
.012	0.30		.290	7.37
.015	0.38		.310	7.87
.020	0.51		.320	8.13
,025	0.64		.330	8.38
.045	1.14		.390	9.91
.060	1.52		1.060	26.92
.065	1.65		1.110	28.19
.090	2.29			
.110	2.79			
.125	3.18			
.140	3.56			
.155	3.94			
.175	4.44			

FIGURE 1. Case outlines Continued.

Case Z



Limits Symbol	Inches		mm	
	Min	Max	Min	Max
A	.060	.080	1.52	2.03
A1	.050	.068	1.27	1.73
b	.022	.028	.559	.711
D	.284	.296	7.21	7.52
D1	.265	.275	6.73	6.99
D2	.150 REF		3.81	
e	.050 ± .005 BSC		1.27 ± 0.13	
E	.484	.496	12.29	12.60
E1	.465	.475	11.81	12.07
E2	.300 REF		7.62	
L	.039	.051	.991	1.30
L1	.395	.405	10.03	10.29
L2	.058	.072	1.47	1.83
L3	.090	.100	2.29	2.54
L4	.065	.075	1.65	1.91
L5	.195	.205	4.95	5.21
R	0.03 REF		0.76	
R1	.012 REF		.305	
R2	.009	.010	.229	.254

FIGURE 1. Case outlines Continued.

Device types	01 through 06	
Case outlines	X, Y, and Z	K
Terminal number	Terminal Symbol	
1	A_5	A_0
2	A_6	A_1
3	A_7	A_2
4	A_8	A_3
5	A_9	A_4
6	A_{10}	A_5
7	A_{11}	A_6
8	A_{12}	A_7
9	A_{13}	A_8
10	$\overline{CE}$	$\overline{CE}$
11	GND	NC
12	$\overline{WE}$	GND
13	I/O_0	$\overline{WE}$
14	I/O_1	I/O_1
15	I/O_2	I/O_2
16	I/O_3	I/O_3
17	A_0	I/O_4
18	A_1	NC
19	A_2	A_9
20	A_3	A_{10}
21	A_4	A_{11}
22	V_{CC}	A_{12}
23	- - -	A_{13}
24	- - -	V_{CC}

NC = no connection

FIGURE 2. Terminal connections.

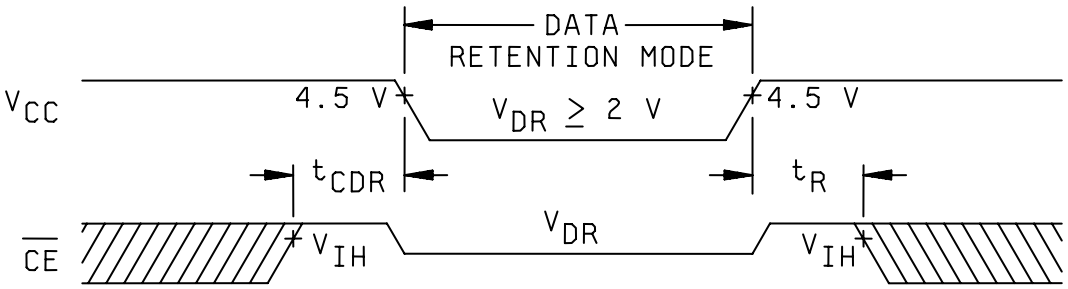
Device types 01 through 06

$\overline{CE}$	$\overline{WE}$	Mode	I/O	Power
H	X	Not selected	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

H = Logic "1" state
L = Logic "0" state
X = Don't care

FIGURE 3. Truth table.

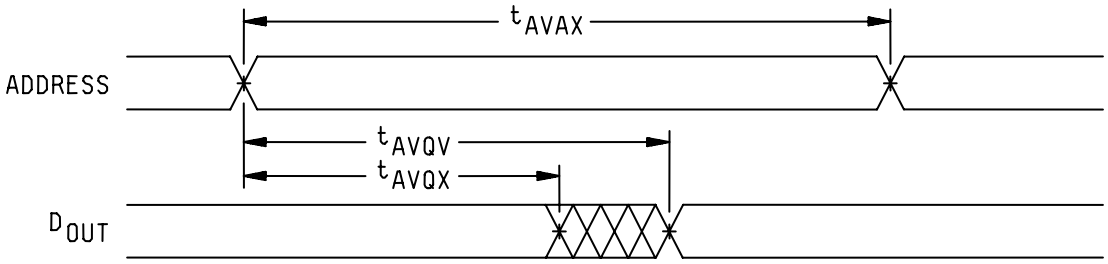
LOW V_{CC} DATA RETENTION WAVEFORM
(DEVICE TYPES 01,03 AND 05)



NOTE: t_{CDR} = 0 ns (minimum); may not be tested, but is guaranteed. $t_r = t_{AVAX}$

FIGURE 4. Switching time waveforms.

TIMING WAVEFORM OF READ CYCLE NO.1



TIMING WAVEFORM OF READ CYCLE NO.2

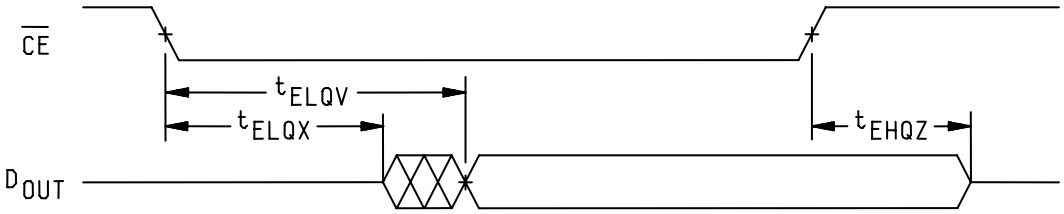


FIGURE 4. Switching time waveforms Continued.

TIMING WAVEFORM OF WRITE CYCLE NO.1

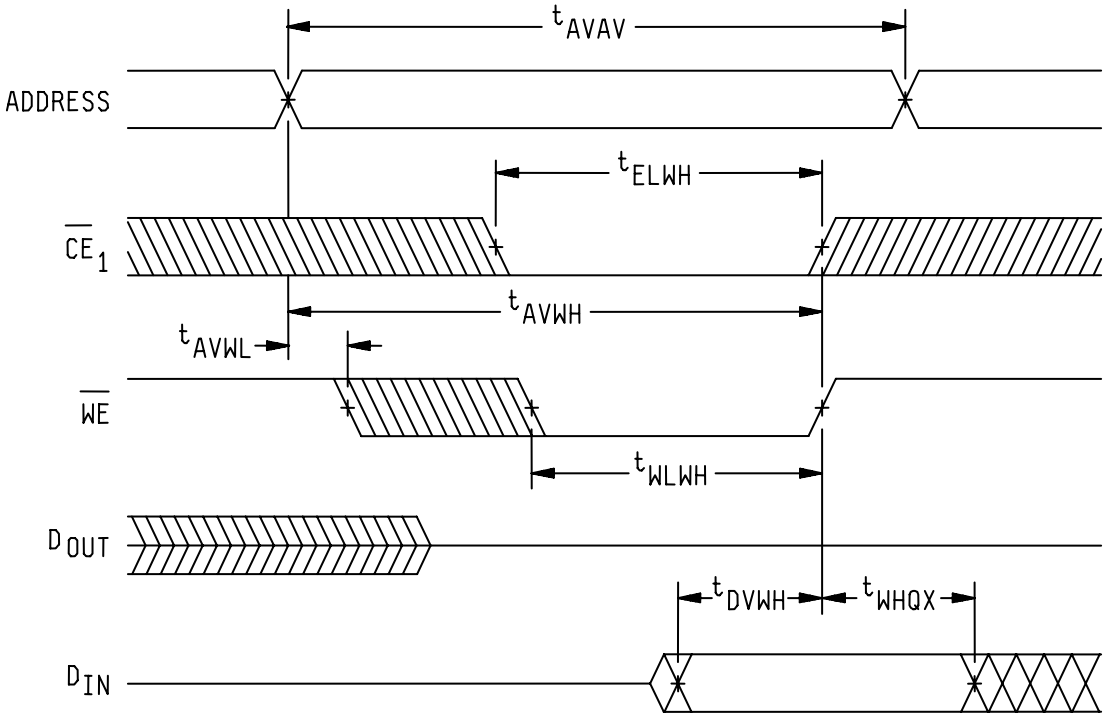


FIGURE 4. Switching time waveforms Continued.

TIMING WAVEFORM OF WRITE CYCLE NO.2

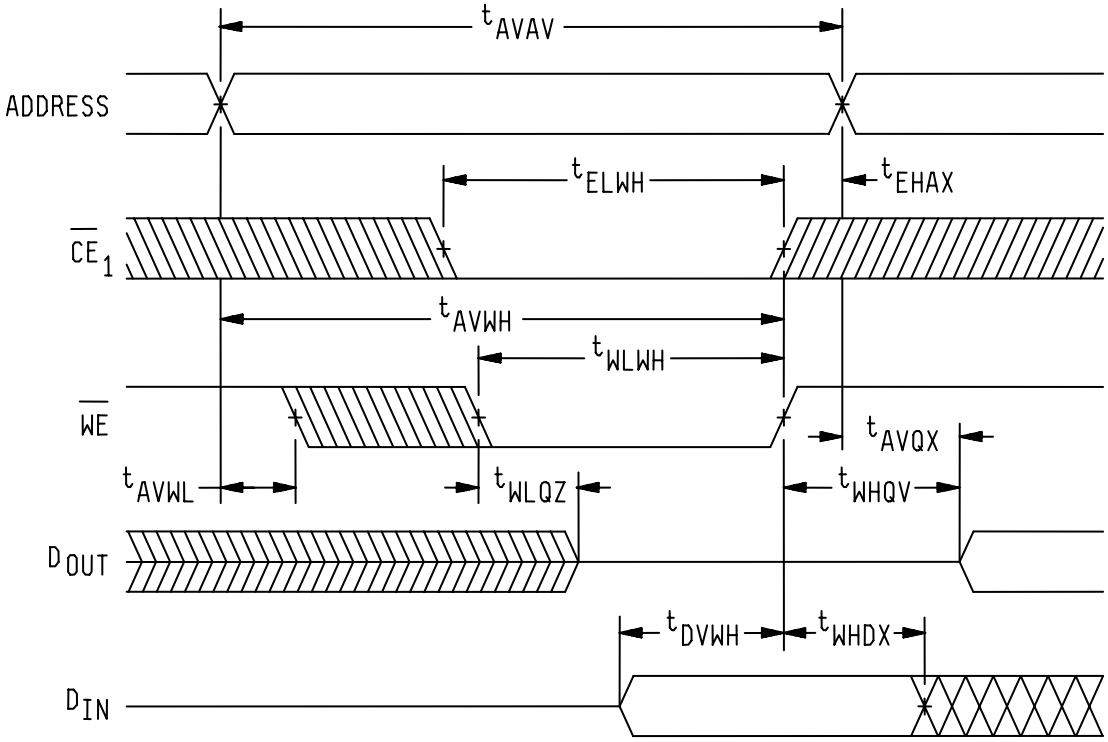
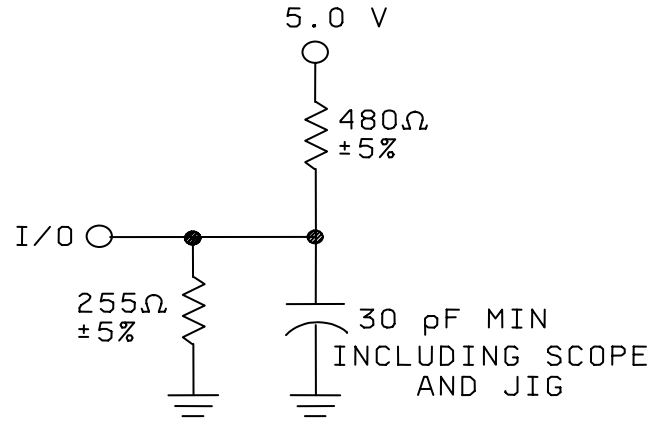
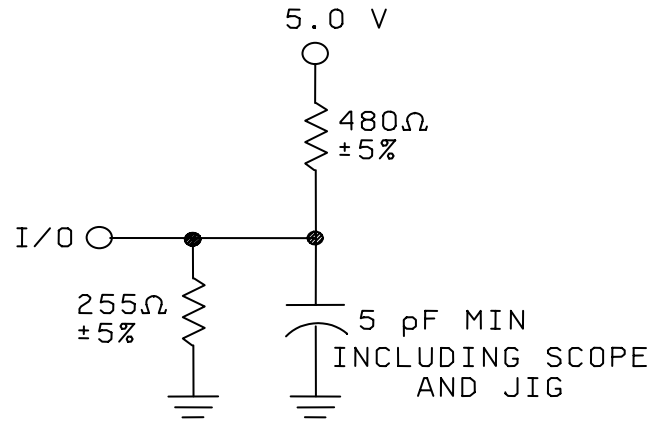


FIGURE 4. Switching time waveforms Continued.



CIRCUIT A OR EQUIVALENT



CIRCUIT B OR EQUIVALENT

FOR t_{ELQX}, t_{EHQZ}, t_{WLQZ} AND t_{WHQV}

FIGURE 5. Output load circuits.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. Subgroups 7, 8A, and 8B tests shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) TA = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7***, (8A, 8B)***, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroup 1.
** See 4.3.1c.
*** See 4.3.1d.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-10-31

Approved sources of supply for SMD 5962-89692 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar part number 2/
5962-8969201KA	3DTT2 3/	P4C188L-25FMB IDT7188L25EB
5962-8969201XA	3DTT2	P4C188L-25CMB
5962-8969201YA	61772 3DTT2	IDT7188L25DB P4C188L-25DMB
5962-8969201ZA	3DTT2	P4C188L-25LMB
5962-8969202KA	3DTT2 3/ 3/	P4C188-25FMB CY7C164A-25KMB IDT7188S25EB
5962-8969202XA	0EU86 3DTT2	MT5C6404C-25883C P4C188-25CMB
5962-8969202YA	3DTT2 61772 3/	P4C188-25DMB IDT7188S25DB CY7C164A-25DMB
5962-8969202ZA	3DTT2 0EU86 3/	P4C188-25LMB MT5C6404EC-25883C CY7C164A-25LMB
5962-8969203KA	3DTT2 3/	P4C188L-20FMB IDT7188L20EB
5962-8969203YA	3DTT2 3/	P4C188L-20DMB IDT7188L20DB
5962-8969203XA	3DTT2	P4C188L-20CMB
5962-8969203ZA	3DTT2	P4C188L-20LMB
5962-8969204KA	3DTT2 3/ 3/	P4C188-20FMB CY7C164A-20KMB IDT7188S20EB
5962-8969204XA	0EU86 3DTT2	MT5C6404C-20883C P4C188-20CMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar part number 1/
5962-8969204YA	3DTT2 3/ 3/	P4C188-20DMB IDT7188S20DB CY7C164A-20DMB
5962-8969204ZA	3DTT2 0EU86 3/	P4C188-20LMB MT5C6404EC-20883C CY7C164A-20LMB
5962-8969205KA	3DTT2 3/	P4C188L-15FMB IDT7188L15EB
5962-8969205YA	3DTT2 3/	P4C188L-15DMB IDT7188L15DB
5962-8969205XA	3DTT2	P4C188L-15CMB
5962-8969205ZA	3DTT2	P4C188L-15LMB
5962-8969206KA	3DTT2 3/	P4C188-15FMB IDT7188-20EB
5962-8969206XA	0EU86 3DTT2	MT5C6404C-15883C P4C188-15CMB
5962-8969206ZA	0EU86 3DTT2	MT5C6404EC-15883C P4C188-15LMB
5962-8969206YA	3DTT2	P4C188-15DMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
3DTT2	Pyramid Semiconductor Corporation 1340 Bordeaux Drive Sunnyvale, CA 94089
61772	Integrated Device Technology, Inc. 2975 Stender Way Santa Clara, CA 95054
0EU86	Austin Semiconductor Inc. 8701 Cross Park Dr. Austin, TX 78754-4566