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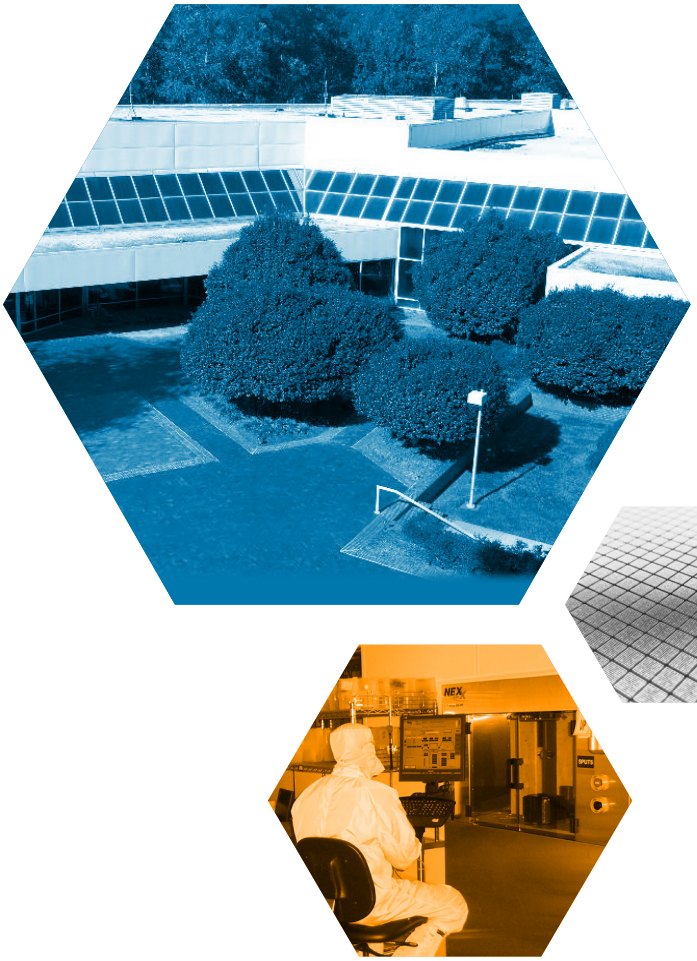
One Source for Innovative Next-Gen Packaging Solutions



Micross Advanced Interconnect Technology supports multiple advanced interconnect and assembly technologies facilitating next-generation electronic systems, including wafer level packaging processes for solder (Pb-based and Pb-free) and Cu pillar bumping, high density (fine pitch) interconnects, through silicon vias (TSV) and silicon and glass interposers. Together, these capabilities support a breadth of 2.5 and 3D heterogeneous integration packaging options.

Micross AIT located in Research Triangle Park, NC, houses an ITAR-registered AS9100D/ISO9001 certified microfabrication facility and has been accredited by the Defense Microelectronics Activity (DMEA) as a Microelectronics Trusted Source for Post CMOS Processing Services (Category 1A).

Micross AIT provides development, custom prototyping and production services as well as unique solutions to challenging interconnect and packaging requirements for a wide variety of commercial, private, government, Defense and Hi-Reliability customers. Our facility supports wafer sizes up to 200mm with established and proven WLP processes and the flexibility to tailor unique solutions for your most demanding interconnect requirements.

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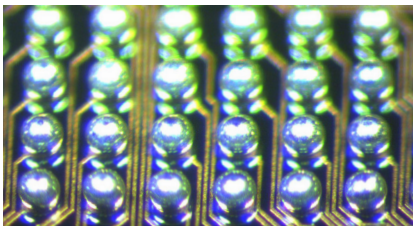
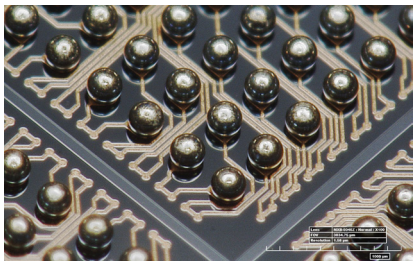
Integration and Advanced Packaging Solutions across a Vast Array of Applications

Micross AIT has been at the forefront of the development of such interconnect and packaging technologies for more than 25 years, making them accessible to external organizations for a wide variety of advanced and low-volume applications. We provide application-based solutions for government and industry clients in technology areas such as high-performance sensor and actuator arrays, biomedical devices and high-performance computing. Some of our integration & packaging technologies include:

- 3D Integration Technology: Through silicon and through glass vias, Si interposers and 3D IC
- Advanced Interconnect and Packaging Technologies Solder bumping, Cu pillar, Cu-based microbumps and assembly

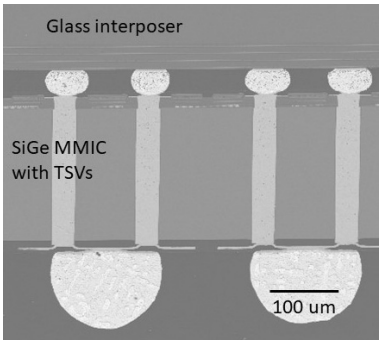




- Microstructure fabrication and packaging: Monolithic integration, novel microfabrication and wafer-level vacuum packaging

Heterogeneous Integration

Micross AIT is a leader in heterogeneous integration technology, having developed a broad range of 2.5D and 3D process capabilities and achieved successful demonstrations of 3D-integrated IC stacks for IR focal plane arrays and silicon interposers for embedded computing modules. We've been developing and implementing heterogeneous integration technologies since 1999, building on decades of experience in the development of advanced microfabrication and packaging technologies.



3D Heterogeneous Integration with TSV, repassivation, redistribution, bumping and assembly

Micross AIT collaborates with a wide variety of clients and partners, bringing integrated process, design, testing and analysis capabilities to projects involving custom application-driven development and access to our 2.5D/3D technology platform through joint development projects, prototyping services and small volume production.

Micross AIT 2.5D/3D integration technology platform is based on several enabling process modules, which include;

- Through-silicon via (TSV) interconnects:
- High density 3D IC applications, filled 2-20 µm diameter, up to 10:1 aspect ratio and
- Wafer thinning (to < 20 µm Si thickness) and processing on temporary carrier wafer
- Flip-chip and high-density metal-metal interconnects and assembly, down to <10 µm pitch
- TSV-last processes for TSV insertion into CMOS device wafers and wafers with high density BEOL metal routing layers

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Wafer Level Packaging

Micross AIT is a leading US-based premier wafer bumping and wafer level packaging facility with 25+ years of experience in developing and providing next-gen interconnect and integration technologies to customers around the world.

Solder Bumping and Wafer Level Chip Scale Packaging (WLCSP)

- WLCSP ball place, electroplated C4, and Cu pillar bumping with bump diameters as small as 25 microns
- Single and multiple layer Cu redistribution with several polymer repassivation material choices
- Eutectic Sn/Pb, Pb-free and high-Pb solder alloys
- Design services and custom test vehicle fabrication

Electronic Material Characterization and Process Development

Micross AIT's extensive experience in flip chip and wafer-level packaging makes us an ideal partner for suppliers developing new materials for advanced packaging, such as photoresists, polymer dielectrics, plating chemistries and underfills.

- Process characterization and optimization
- Implementation into full process flows
- Test vehicle fabrication and reliability testing

Flip Chip and Multi-Chip Module Assembly

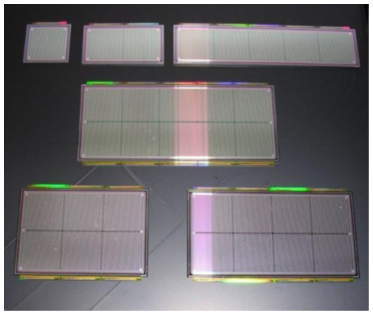
From single chip placements to multi-chip module and system-in-package assembly of multiple die and components, we offer a wide array of capabilities:

- Flip chip assembly for single & multi-chip applications
- Precision die placement with accuracies better than +/- 0.5 microns
- Heterogeneous integration with Si, III-V, and other device types
- Plasma Assisted Dry Soldering (PADS) Process enables true fluxless for assembly for Sn-bearing solders

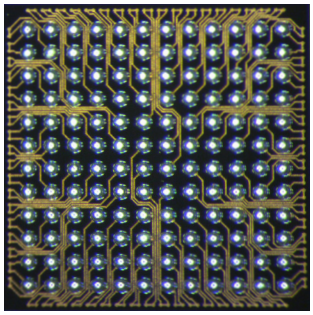
Metal-Metal Bonding for 2.5/3D Technologies

- 2.5D and 3D integration technologies are driving the integration of devices with extremely high interconnect densities for Si interposer and chip stacking applications.
- Solid/liquid interdiffusion assembly with CuSn-Cu bump arrays demonstrated down to 10 micron pitch
- Cu/Cu thermocompression bump bonding demonstrated down to 5 micron pitch
- Solutions for chip stacking and high thermal stability interconnects that remain stable at high temperatures

Customers can take advantage of the 2.5D/3D integration technology platform to realize more highly integrated microsystems with increased functionality, short interconnect length and decreased size, weight and power (SWaP). From design and fabrication of custom test vehicles to application of 3D integration processes modules on fully functional IC wafers, Micross AIT can provide a variety of integration solutions to meet specific project needs.



Flip Chip & Multi-Chip Module assembly



Wafer Bumping

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Contact AIT to learn more about how we can provide the most optimized solution for your system or application:

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